UNIVERSITY OF CAMBRIDGE

Solid State Devices

4B6

Lecture 6 – TFT technology

Daping Chu

Lent 2016

Macroelectronics for large areas

EPSON 40in OLED TV, reported by NHK Oct 2004

Larger size
Faster speed
Higher current

Macroelectronics for large areas

Traditional microelectronics:

Silicon wafer (12in) based

MOSFETs

Objectives:

- Smaller geometry
- Higher speed
- Higher device density

  DRAM, Flash, FRAM, ...
- Lower power consumption

Large area macroelectronics:

Alternative substrate (3m) based

Thin-film transistors (TFTs)

Objectives:

- Larger area
- Higher speed and higher current
- Higher resolution

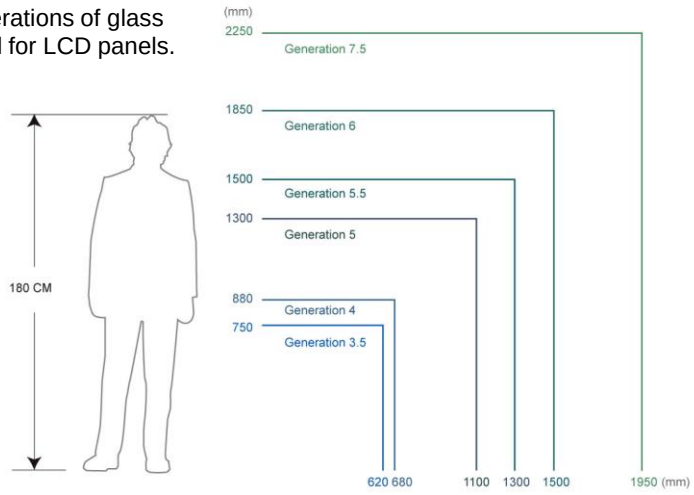
  VGA (640x480), ..., to

  UXGA (1600X1200, 4:3), ...

  WUXGA (1920X1200, 16:9), ...
- Lower power consumption

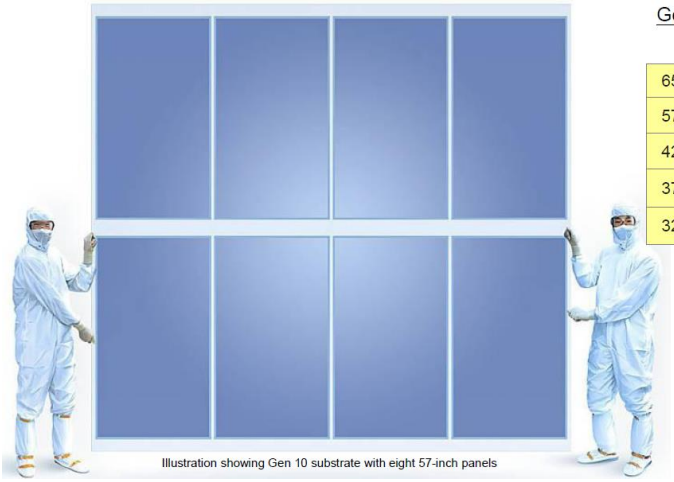
Macroelectronics for large areas

Generations of glass panel for LCD panels.



Oct 2009, Sharp Gen-10 (2850x3050mm^2) production. Fab costs US$4.25b.

Macroelectronics for large areas



Gen 10 panelization

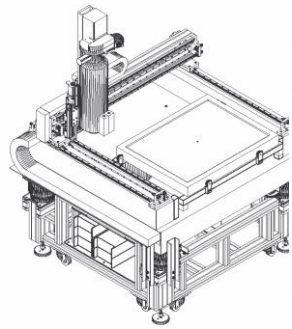
	Panel #	Efficiency
65"	6	84%
57"	8	86%
42"	15	89%
37"	18	84%
32"	24	84%

CORNING

Full HDTV 42" 1080p (1920x1080 pixels) ➔ >31m TFTs on a Gen-10 substrate

Macroelectronics for large areas

Automated optical inspection tool for LCD panels



Specifications	X Stage	Y Stage
Length (mm)	1600	900
Moving mass (Kg)	130	60
Accuracy (µm)	± 50	± 50
Repeatability (µm)	± 25	± 25
Max speed (m/s)	0.8	0.7
Moving time (full range) (s)	3	2

- Two faulty pixels ➔ 2nd Grade panel.
- Strong requirement on the production yield of the TFTs for **uniformity** and **reliability**.

TFT history


J. Lilienfeld


O. Heil


W.E. Spear


P.G. LeComber

TFT Invention
1933-34

1960's
First TFT
(CdS)

P.K. Weimer
(RCA Labs)

a-Si TFT
1970's

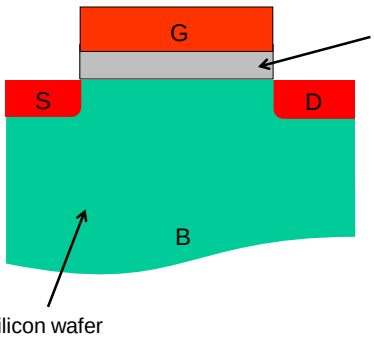
1980's
Poly-Si TFT

Organic TFT
1990's

2000's
Transparent
metal oxide
TFT

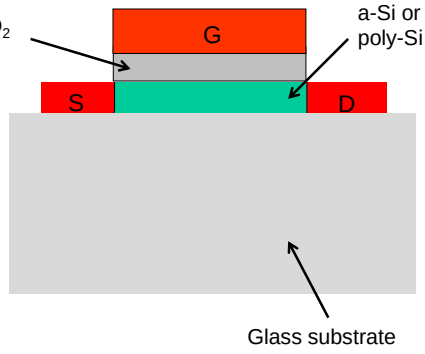
Silicon MOSFET vs Silicon TFT

<u>Silicon MOSFET</u>



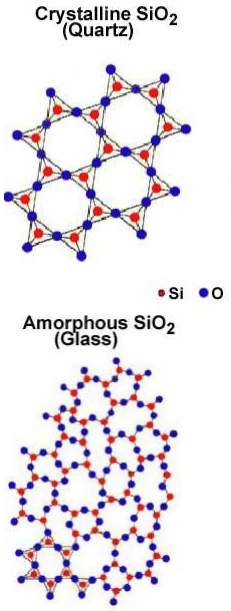
Doped channel.
Potential profile fixed by biases.

<u>Silicon TFT</u>

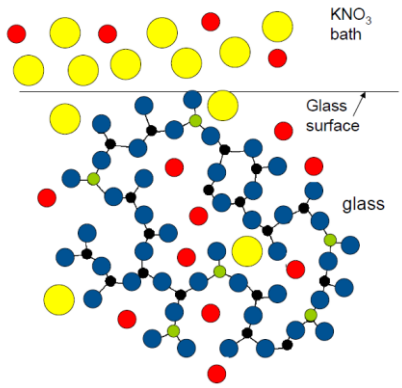


Undoped channel.
Floating body effect at transient.
(speed can be limited by this,
especially for long channel devices.)

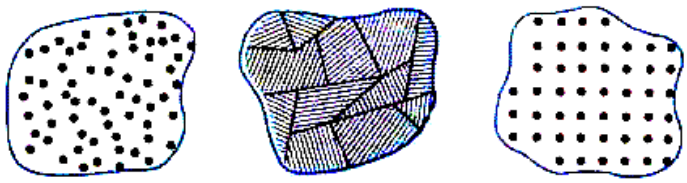
Materials

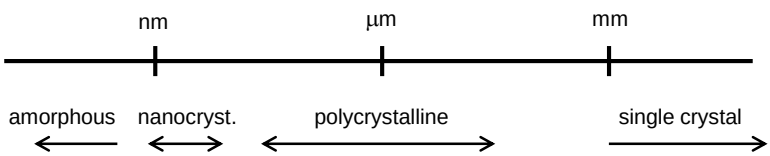


Alumino-silicate thin sheet glass prepared by ion-exchange process for high strength and reliability.



Materials





Materials

Traditional method to grow poly-Si films:

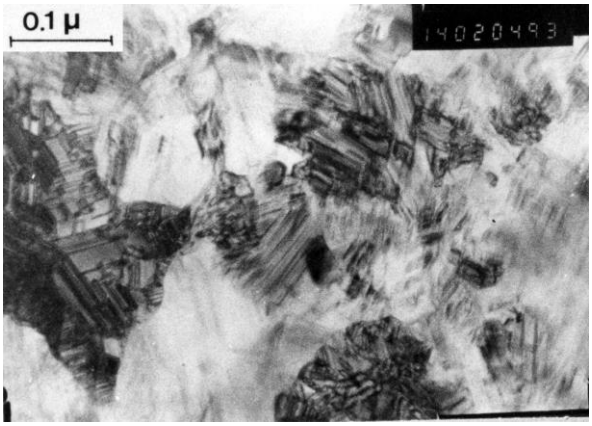
Low Pressure Chemical Vapour Deposition (LPCVD), SiH_4, 625°C

$$SiH_4 \xrightleftharpoons{625\ ^\circ C} Si + 2H_2$$

Low pressure: 0.5-1 torr;
Material too defective, electron mobility < 5 cm^2/Vs

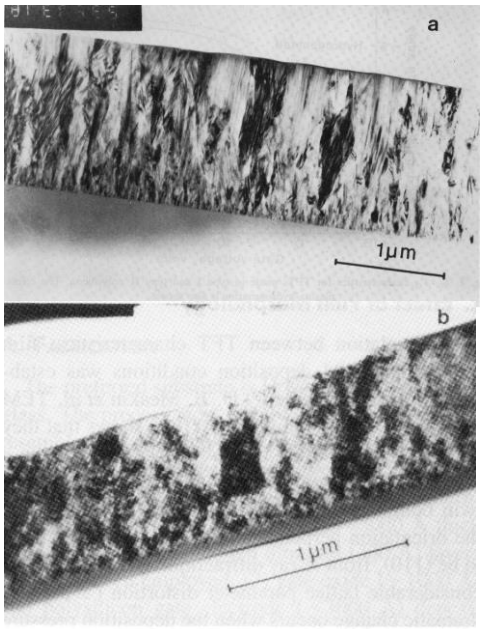
Low pressure: 0.01-0.04 torr;
Improved material, electron mobility 15-30 cm^2/Vs
(Meakin et al., GEC,1986; Miyasaka et al. Epson, 1991)

Materials



Normal TEM
LPCVD, Deposition Pressure 0.5torr.

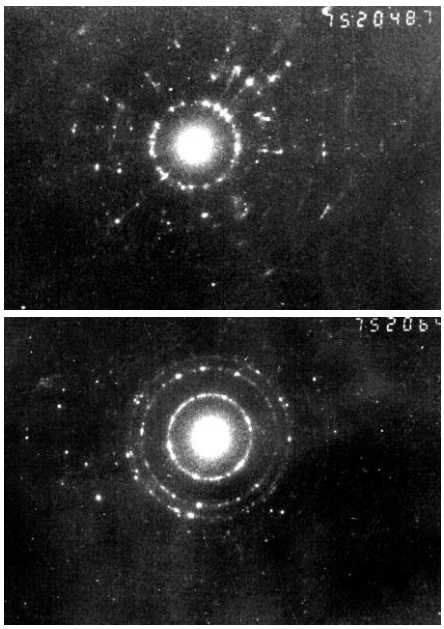
Materials



Cross section TEM
LPCVD, Deposition Pressure 0.5torr.

Cross section TEM
LPCVD, Deposition Pressure 0.04torr.

Materials



LPCVD, Deposition Pressure 0.5torr.
Significant lattice distortion.

LPCVD, Deposition Pressure 0.04torr.
Minimum lattice distortion.

Materials

Correlation between microtwinning and lattice parameter distortion:
(Meakin et al., GEC, 1986)

LPCVD poly-Si deposited at normal pressure (0.5 torr):

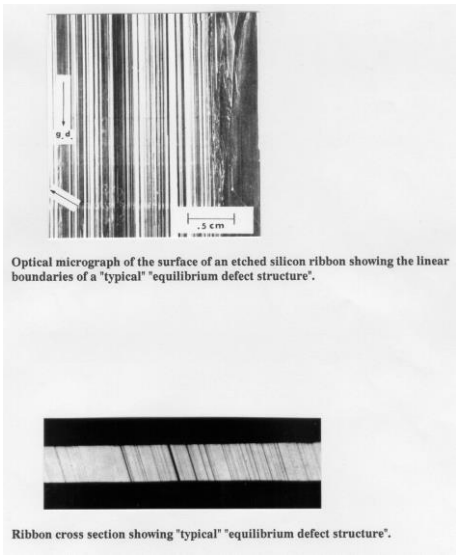
- many microtwins;
- large lattice parameter distortion; (~3%)
- Poor TFT performance.

LPCVD poly-Si deposited at reduced pressure (<0.04 torr):

- fewer microtwins
- no lattice parameter distortion;
- improved TFT performance.

Materials

Coherent twins in silicon ribbon



Optical micrograph of the surface of an etched silicon ribbon showing the linear boundaries of a "typical" "equilibrium defect structure".

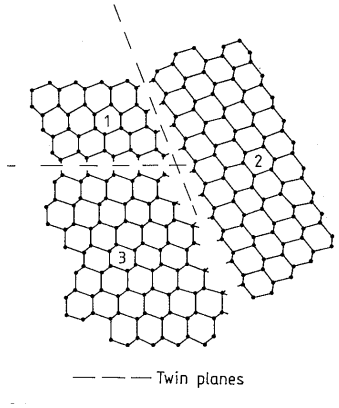
Ribbon cross section showing "typical" "equilibrium defect structure".

Coherent twins are electrically inactive.

Materials

Coherent boundaries: 1-2 and 1-3

Incoherent boundary: 3-2



When 3 twins are randomly oriented incoherent boundaries may occur.

Along the 3-2 interface TWO bonds on 3 face ONE bond on 2, resulting in:

- **dangling bonds;**
- **lattice parameter distortion.**

Materials

Present method to fabricate poly-Si film:

Amorphous silicon deposition followed by re-crystallisation

Deposition methods:

- Plasma Enhanced Chemical Vapour Deposition
  from SiH_4
- Low Pressure Chemical Vapour Deposition
  from Si_2H_6 450°C

Crystallisation methods:

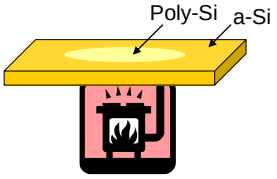
- Thermal nucleation and growth (SSC);
- Melting, nucleation and growth (RTA, ELA);
- Metal induced lateral growth (MILC).

Objective:

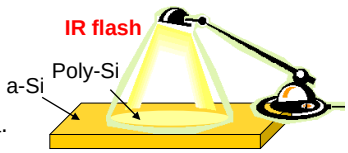
Minimise structural defects.

Materials

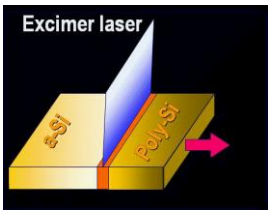
Solid state crystallisation (SSC)
- Small size grains but more uniform.
- Low fabrication cost.
- Slow and high temperature, not really suitable for glass substrates.



Rapid thermal annealing (RTA)
- Medium size grains but not very uniform.
- Medium fabrication cost.
- Decrease in yield for increase of heating area.

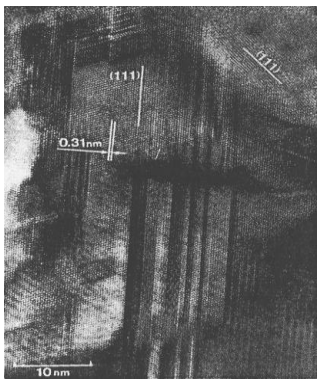


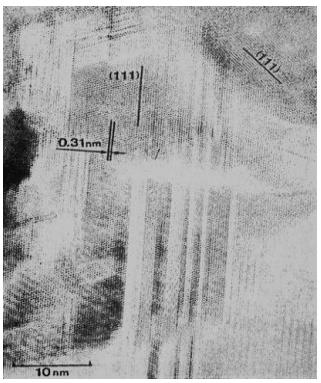
Excimer laser annealing (ELA)
- Large size grains but not uniform.
- High fabrication cost.
- Decrease in yield for increase of scanning size.



Materials

Poly-Si film produced by thermal recrystallisation (SSC) at 600ºC for 20hrs

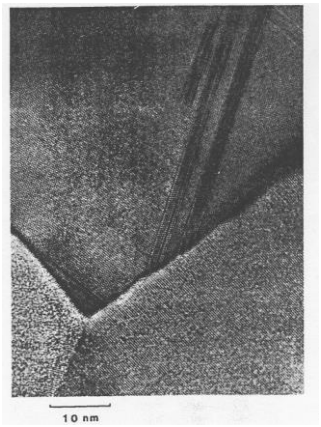


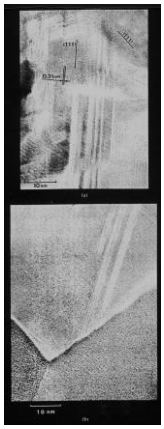


Under subsequent high temperature treatment,
(e.g oxidation at 950ºC)
planar defects such as microtwins or stacking faults anneal out.
This material is suitable for high temperature TFTs on quartz,
as used in LCD projectors.

Materials

Laser re-crystallisation:





thermal

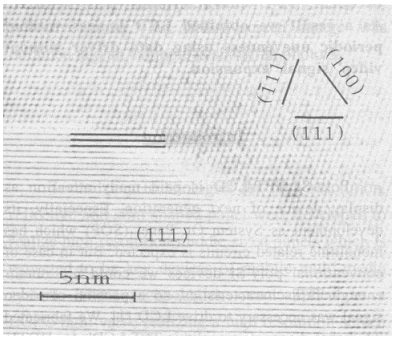
laser

Sharp grain boundaries;
Reduced intra-grain defect concentration.

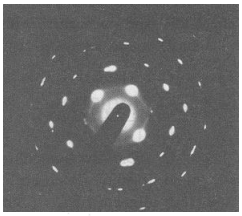
Materials

Continuous-grain silicon technology
(Ohtani, et al., Sharp, 1998)

HRTEM image of grain boundary



Electron diffraction image (1.35x1.35μm²)

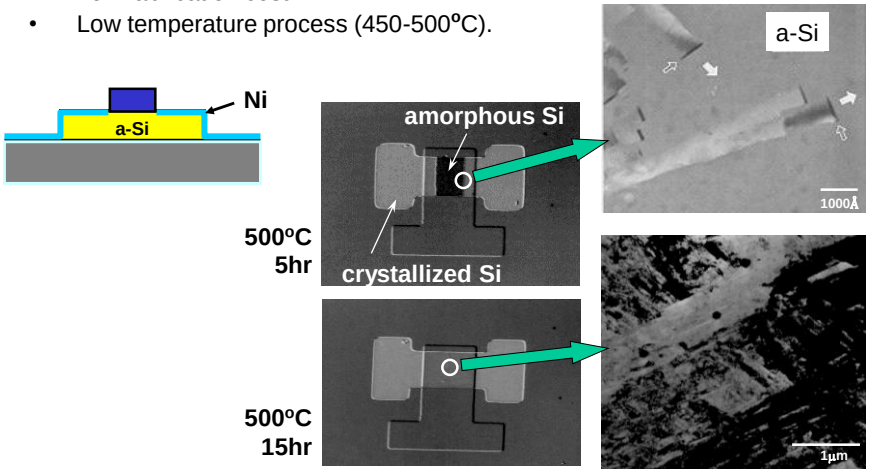


Channel Type	Vth [V] ($\|V_D\|$=5V)	S-value [mV/dec] ($\|V_D\|$=1V)	μ_{FE} [cm^2/Vs] ($\|V_D\|$=1V)
N	0.12	74.4	317.7
P	-1.00	76.1	140.6

Materials

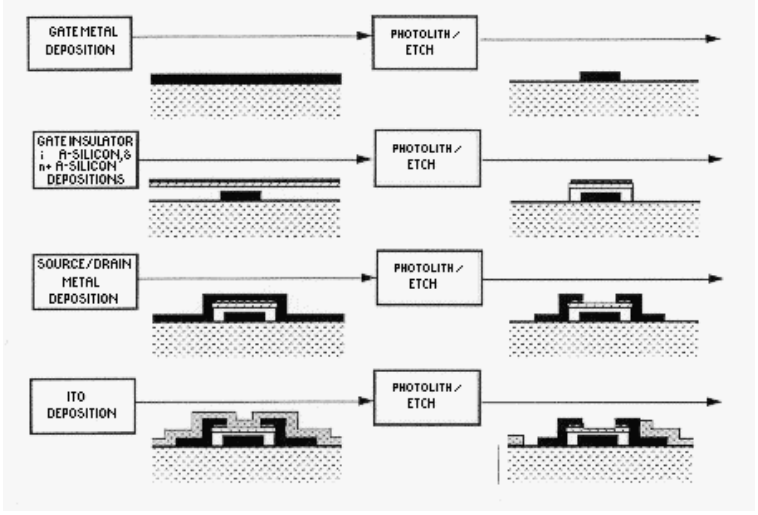
Metal induced lateral crystallisation (MILC)

- Ni or Pd deposited on a-Si film and selective crystallisation.
- Low fabrication cost.
- Low temperature process (450-500°C).

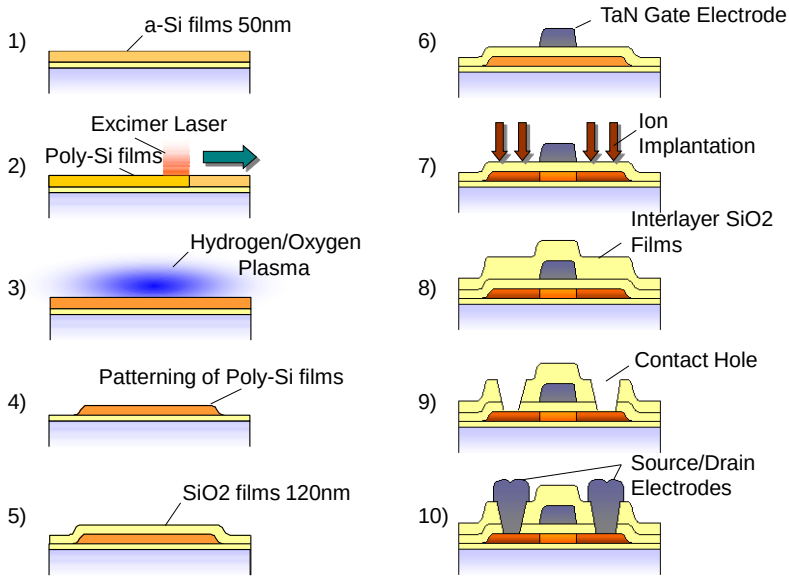


Seung-Ki Joo

Fabrication process – a-Si TFT

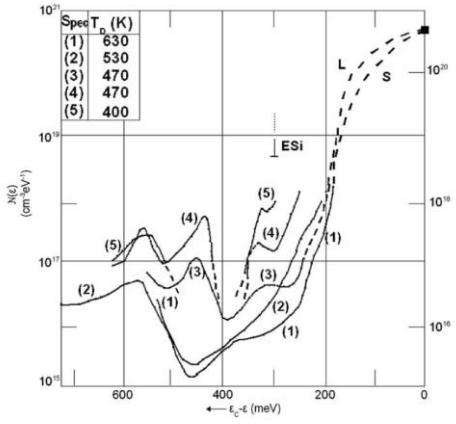


Fabrication process – Poly-Si TFT



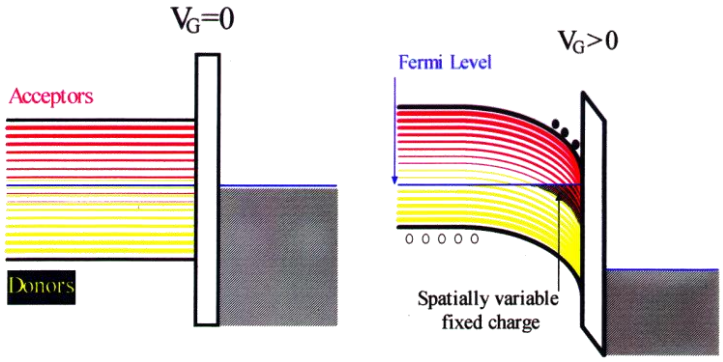
Localised density of states in the band gap

The density of localised states, N(E), plotted against the energy Ec–E for a number of a-Si samples produced using the 'glow discharge' (or PECVD) technique in SiH_4 gas. T_D is substrate temperature during deposition.



W.E. Spear, P.G. LeComber, J. Non-Cryst. Solids 8–10 (1972) 727.

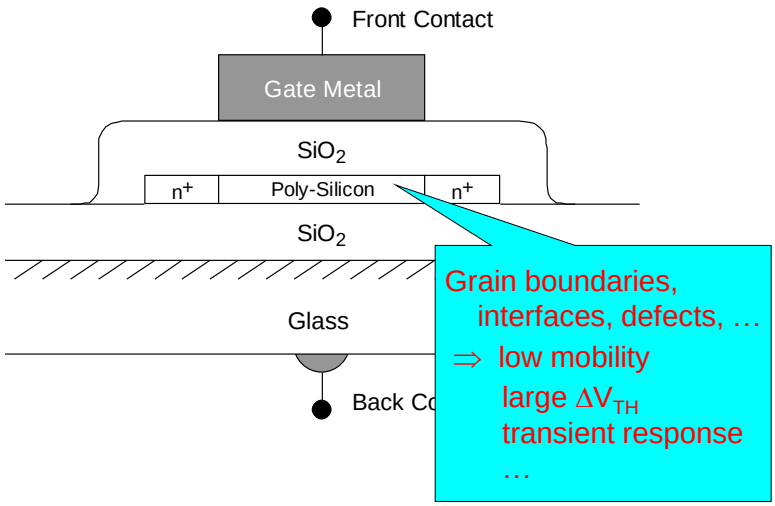
Localised density of states in the band gap



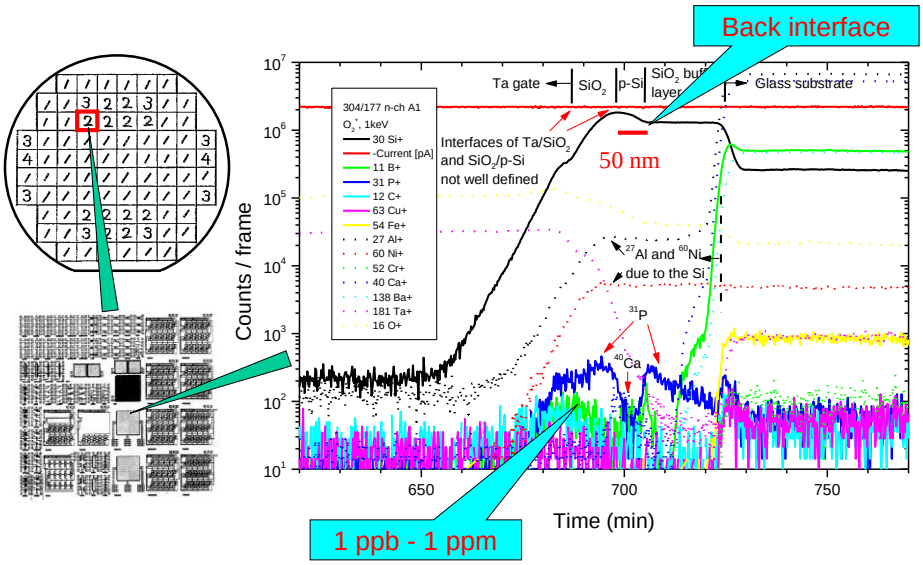
There are continuous localised states within the band gap for BOTH a-Si and poly-Si films (due to defects, impurities, unsatisfied bonds, grain boundary states, interface states, etc), which can be empirically fitted by:

$$N(E) = N_{at} e^{\frac{E-E_C}{E_{at}}} + N_{ad} e^{\frac{E-E_C}{E_{ad}}} + N_{dt} e^{\frac{E_V-E}{E_{dt}}} + N_{dd} e^{\frac{E_V-E}{E_{dd}}}$$

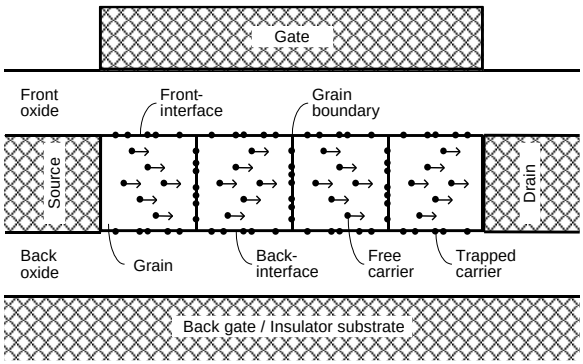
Poly-Si TFT



Poly-Si TFT



Poly-Si TFT

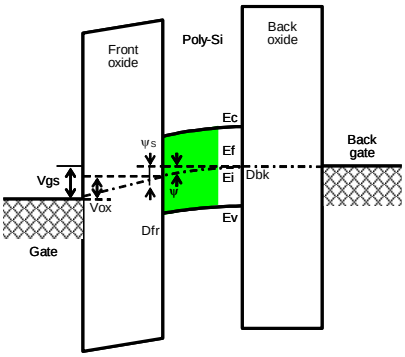


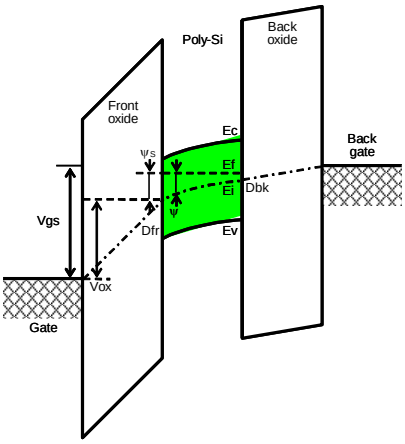
Charge carrier transport is considerably affected by grain boundary (GB).

Different GB number ➔ Different TFT performance!

Statistical fluctuation for short channel TFTs made by using large size grains.

Poly-Si TFT

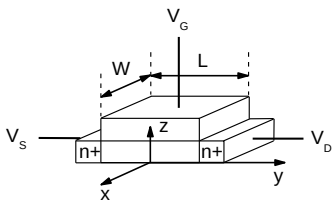




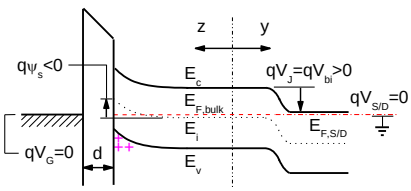
Channel partially depleted (PD)
Channel depth < Film thickness
Only front interface scattering

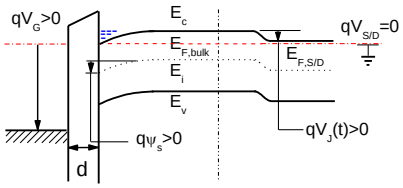
Channel fully depleted (FD)
Channel depth = Film thickness
Both front and back interface scattering

Poly-Si TFT



Poly-Si channel with
n-type source and drain

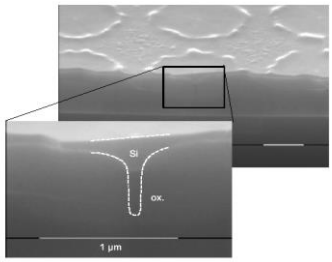


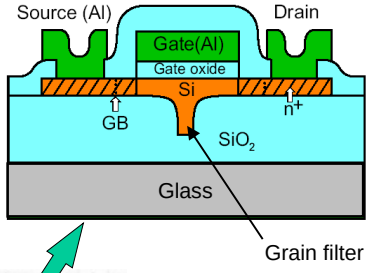


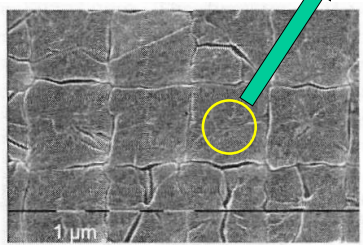
$V_G = V_S = V_D = 0$
Front interface states

$V_G > 0$, $V_S = V_D = 0$
Partially depleted channel

Poly-Si TFT



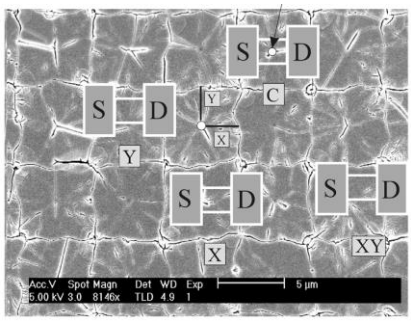




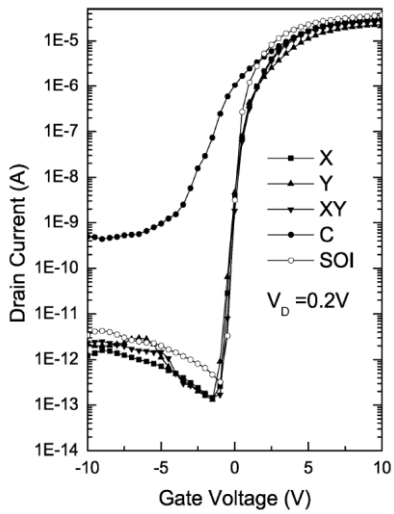
Grain filter

Single grain TFT using laser annealing with a pre-patterned filter for seeding arrangement. Very good registration.

Poly-Si TFT



TFTs	Channel position	μ_{FEe} (cm^2/V-s)	S (V/dec.)	I_{OFF}* 1E-13(A)	V_{TH} (V)
Grain-filter	X	597± 101	0.21± 0.03	1.3± 0.5	1.7± 0.2
	Y	528± 57	0.25± 0.04	1.7± 0.8	1.8± 0.3
	XY	505± 55	0.22± 0.01	1.4± 0.1	1.9± 0.1
	C	471± 32	1.1± 0.13	16800± 16900	0.86± 0.3
SOI		727±18	0.18± 0.006	3.57± 0.26	1.1± 0.09

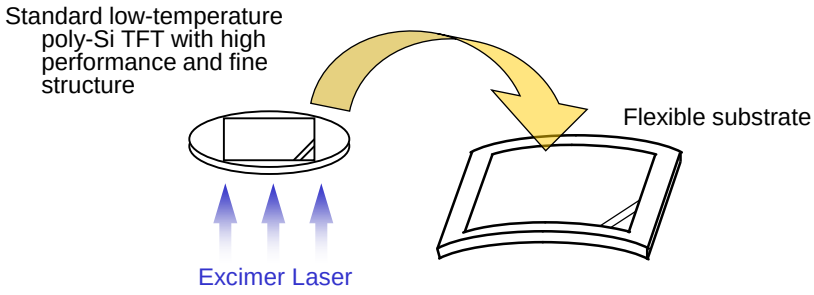


L=W=2μm, with 250nm thick silicon layer and a 120-nm gate insulator.

Rana, et al., Delft/Epson, 2005

Poly-Si TFT

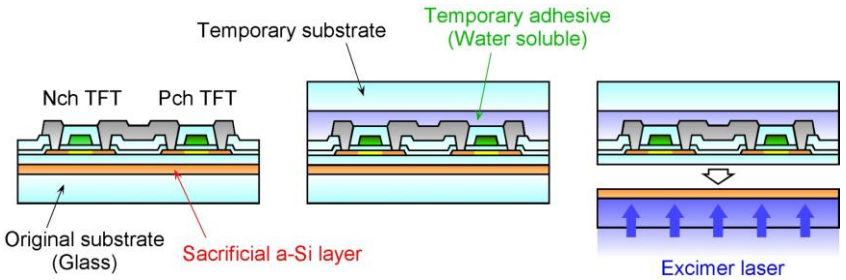
SUFTLA®
(Surface Free Technology by Laser Ablation / Annealing)
EPSON



Transfer of single grain TFTs possible.

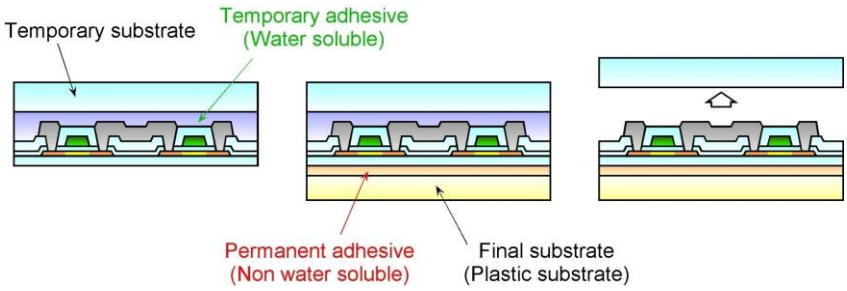
Poly-Si TFT

SUFTLA®
(Surface Free Technology by Laser Ablation / Annealing)
1st Transfer Step



Poly-Si TFT

SUFTLA®
(Surface Free Technology by Laser Ablation / Annealing)
2nd Transfer Step



Poly-Si TFT

SUFTLA®
+
E-ink

EPSON (Jun 2006)
A6 (7") (397dpi)

Silicon MOSFET vs Silicon TFT

	Si MOSFET	a-Si:H TFT	Poly-Si TFT
Design Rule	< 45 nm	10-20 μm	5-10 μm
Mobility	1500 cm^2/Vs	1 cm^2/Vs	100 cm^2/Vs
Device Type	n- & p-type	n-type	n- & p-type
Substrate	Si wafer	Glass	Glass / Quartz
Process Temperature	1000 ˚C	300 ˚C	450 - 700 ˚C
Process Technology	Photolithography	CVD deposition Photolithography	CVD deposition Crystallisation Photolithography
Interconnects	Multi-metal layers	One metal layer	>1 Metal layers
Reliability	High	Low	Medium
Uniformity	High	High	Medium
Cost/Area	High	Low	Medium

Silicon MOSFET vs Silicon TFT

Silicon MOSFETs:

High speed and high density for CPU (GHz), Memory (Gb) and alike,
But area is limited by wafer size.

a-Si TFTs:

Active matrix backplane for LCD TVs and alike,
Speed and current limited mainly by channel mobility,
Life time limited by material instability,
Uniform TFT performance over large area,
But transistors suffer from degradation in performance due to bias stress.

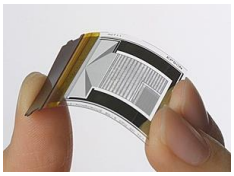
High temperature poly-Si (HTPS) TFTs:

Active matrix backplane for LCD projectors and alike,
Higher speed and current than a-Si TFTs,
Better life time and much less bias stress degradation,
But area and costs are limited by high temperature substrates such as quartz.

Low temperature poly-Si (LTPS) TFTs:

Active matrix backplane for OLED and alike,
Much higher speed and current and suitable for most applications,
But **production yield is limited by transistor uniformity over large area**.

Poly-Si TFT System-on-Panel



8-Bit Asynchronous Microprocessor
Using poly-Si TFTs
(EPSON, Feb 2005)

All parts can be made by using poly-Si TFTs.