UNIVERSITY OF CAMBRIDGE

Solid State Devices

4B6

Lecture 9/10 – MRAM

Daping Chu

Lent 2016

Giant Magneto Resistance

Introduction

Giant Magneto Resistance (GMR)
- – Basic structure and GMR effect
- – Definition of magneto-resistance MR%
- – Performance of a GMR superlattice
  - Dependence of exchange coupling on spacer thickness
- – Comparison of configurations
  - Current-perpendicular-to-plan (CPP)
  - Current-in-plan (CIP)

The Nobel Prize in Physics 2007

KUNGL. VETENSKAPSAKADEMIEN
THE ROYAL SWEDISH ACADEMY OF SCIENCES

Useful Links / Further Reading

The Nobel Laureates

Albert Fert, Unité Mixte de Physique CNRS/ THALES, Université Paris-Sud

Peter Grünberg, Forschungszentrum Jülich GmbH

Scientific review articles

"Giant steps with tiny magnets" by Agnes Barthélémy and Albert Fert et al., Physics World Nov. 1994.37

"Spintronics" by Dirk Grundler, Physics World April 2002.

Original scientfic articles

"Giant Magnetoresistance of (001)Fe/(001)Cr Magnetic Superlattices" by M.N. Baibich et al., Physical Review Letters Vol. 61, No. 21 (1988). (Albert Fert's original article)

"Enhanced magnetoresistance in layered magnetic structures with antiferromagnetic interlayer exchange" by G. Binasch et al., Physical Review B, Vol. 39, No. 7 (1989). (Peter Grünberg's original article).

Giant Magneto Resistance

GMR and basic structures

Magneto-resistance MR%:

$$\mathrm{MR\%} = \frac{\Delta R}{R}(\%) = \frac{\Delta \rho}{\rho}(\%)$$

GMR: ΔR/R as high as 50% (Rm Temp)

Normal MR: typical materials << 5%

Three essential elements to get the GMR effect

Two ferromagnetic (FM) metal layers

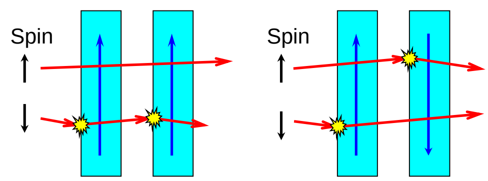
One non-magnetic layer

Giant Magneto Resistance

Two ferromagnetic metal layers

Ferromagnetic + Metallic

- Electrons in the metal conduction band ➔ Conduction
- Spin of the electrons ➔ Magnetisation
- Difference of spin-related electron populations ➔ GMR
  (∵ different scattering cross-sections
  between ↑↑ and ↑↓)

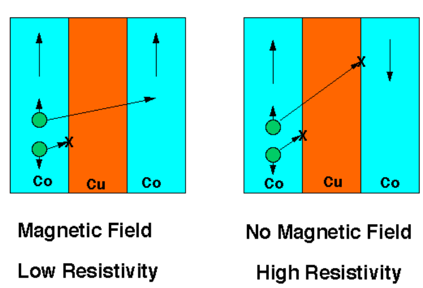


Giant Magneto Resistance

One non-magnetic layer

The Spacer

- Separation between the two FM layers
  ➔ Strength of exchange coupling
- Conductive spacer ➔ Spin Valve, Pseudo-Spin Valve
- Insulating spacer ➔ Magnetic Tunnel Junction



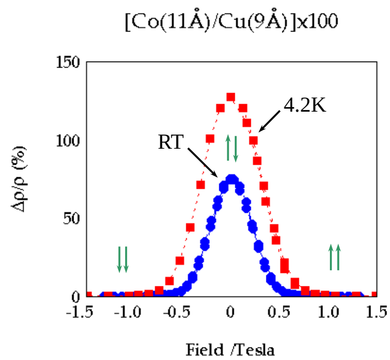
Giant Magneto Resistance

MR definition and a GMR device

Definition of MR%:

$$\mathrm{MR}\% \equiv \frac{R(\mathrm{AP}) - R(\mathrm{P})}{R(\mathrm{P})} \times 100 = \frac{\Delta R}{R}(\%) = \frac{\Delta \rho}{\rho}(\%)$$

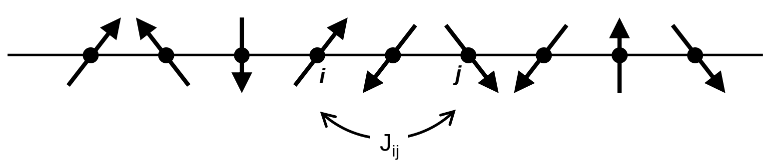
A GMR device:
(superlattice)



Giant Magneto Resistance

Magnetic coupling

For two magnetic moments, $\mathbf{M}_i$ and $\mathbf{M}_j$, at site *i* and *j*,



the energy of magnetic interaction between them is:

$$E_{ij} = -J_{ij}\mathbf{M}_i \bullet \mathbf{M}_j$$

where J_{ij} is the exchange coupling between these two sites.

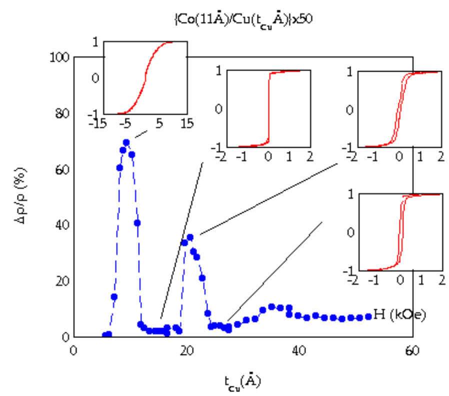
$J_{ij} > 0$ ➔ Ground state is Ferromagnetic (FM)
$J_{ij} < 0$ ➔ Ground state is Anti-Ferromagnetic (AFM)

Giant Magneto Resistance

Spacer thickness effect

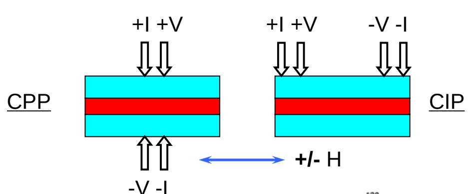
Exchange coupling depending on spacer thickness:
– RKKY type exchange interaction

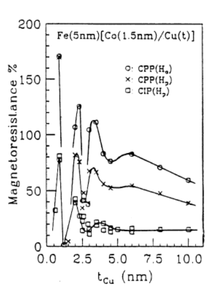
$$J_{RKKY} \propto \frac{\cos(2k_F r)}{(2k_F r)^3}$$

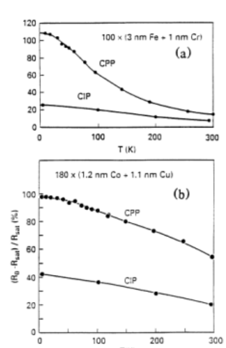


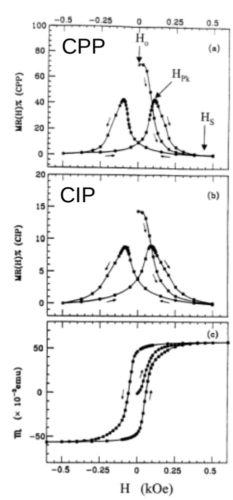
Giant Magneto Resistance

CPP vs CIP









$[Co(6nm)/Ag(6nm)]_{60}$ at 4.2K

Spin valve

Introduction

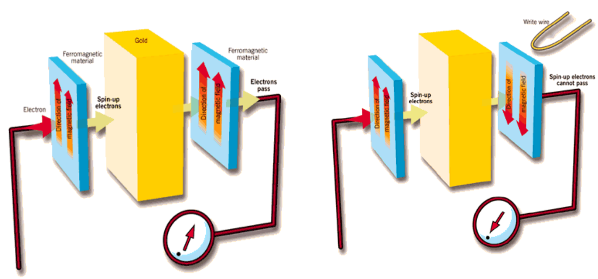
Spin valve (SV)
- Basic structure and pinning
- Different pinning approaches and performances
- Spin valve MRAM arrays
    - 1T or 1D?
        - How to write
- An example
    - 1D SV cell

Spin valve

Basic structure

Direction of magnetization: **fixed** (pinned) in one FM layer;
free to switch in the other one.
Spacer is conductive.

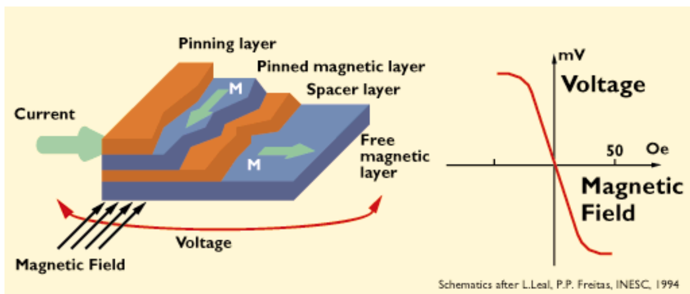
Different levels of MR when parallel/antiparallel ➔ "0"/"1”



Spin valve

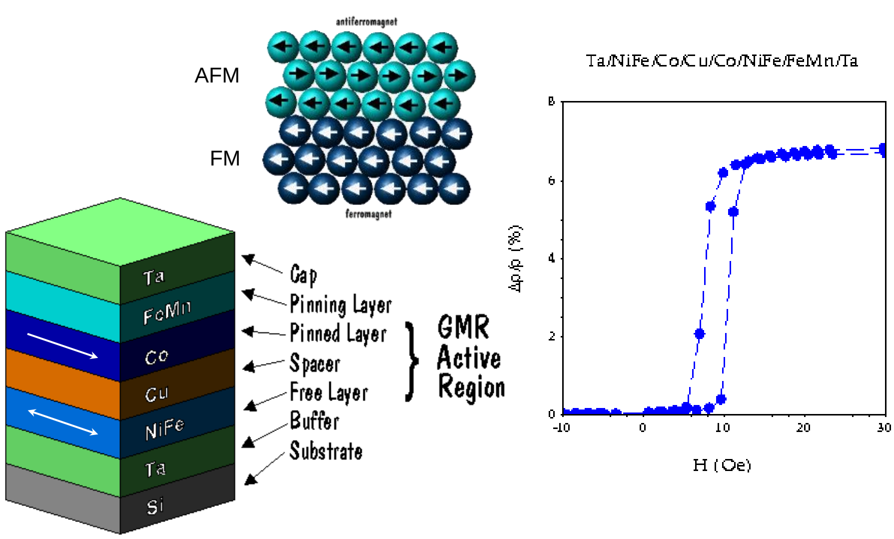
Pinning

Fixed direction of magnetization through a strong magnetic coupling between the pinning layer and pinned layer.



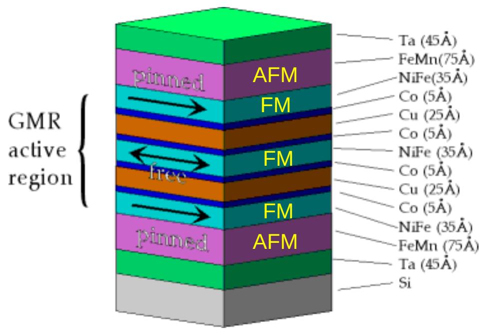
Spin valve

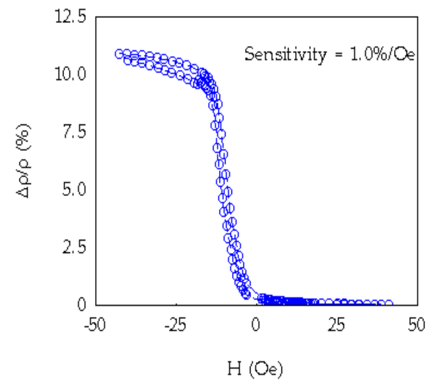
Top pinning



Spin valve

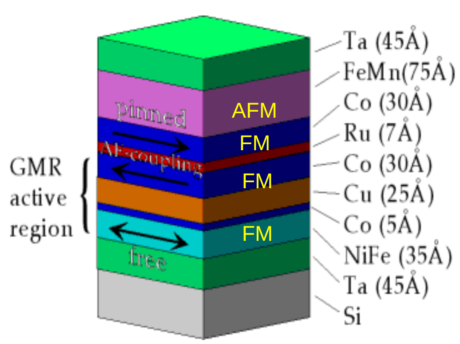
Symmetric pinning

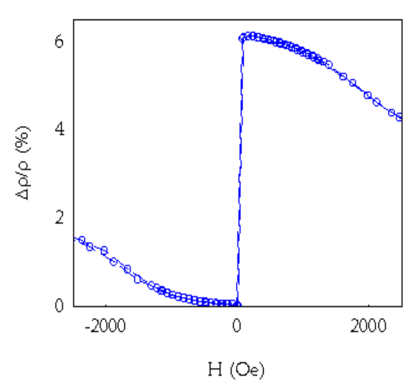




Spin valve

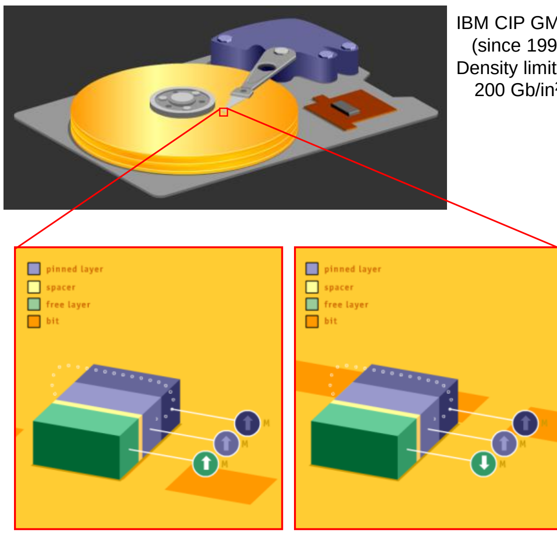
Antiferromagnetic coupling pinning





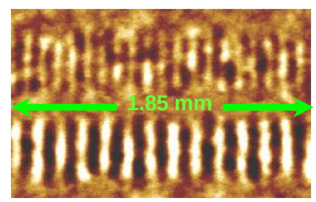
Spin valve

CIP spin valve GMR head



IBM CIP GMR head
(since 1997)
Density limit:
200 Gb/in^2

3 GMR nanosliders on a US quarter.

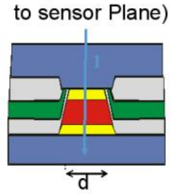


Two written tracks made by IBM:
Upper track density 35 Gb/in^2
Lower track density 23 Gb/in^2

Spin valve

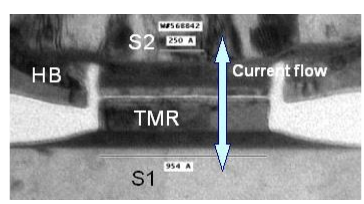
CPP spin valve GMR head

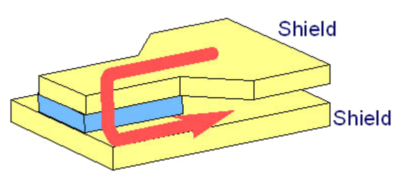
CPP (Current Perpendicular to sensor Plane)



Area A ~ d^2

$R_{SENSOR} = R_j\ (\Omega\text{-}\mu m^2) / A$





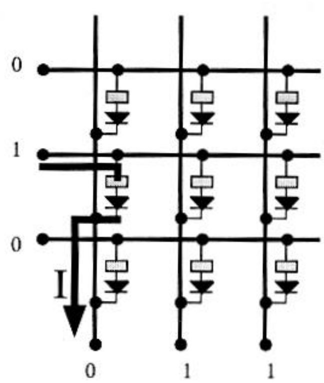
Hitach CPP GMR head
(Oct 2007)
Density expected:
500 Gb/in^2 to 1 Tb/in^2

By 2011: 1 Tb HDD for laptop
4 Tb HDD for desktop

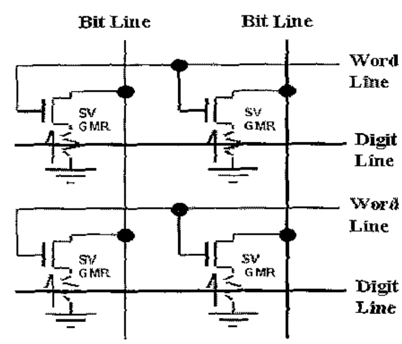
Spin valve

1D/1R and 1T/1R arrays

1D/1R



1T/1R

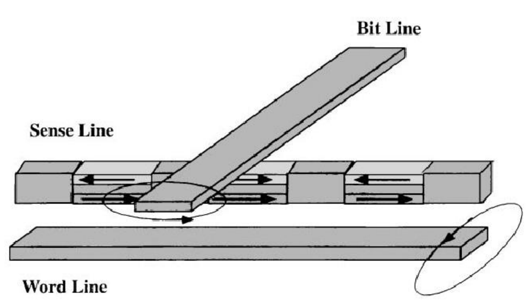


Spin valve

Read is easy, how to write?

The technique to avoid the mis-write due to the half-selection:

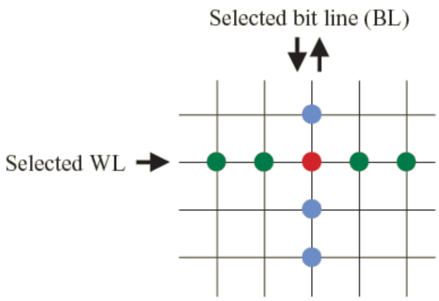
- Send a pulse to word line, switching the cells half way;
- Send another pulse to bit line to complete the switch;
- Only the **combined** field is strong enough to switch the free layer of the selected cell.

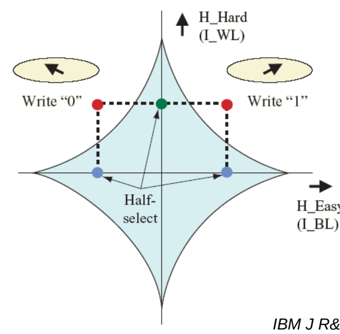


Spin valve

Coincident field selection

Coincident field selection and switching threshold (asteroid) curve for writing a magnetic element of an MRAM. The ellipses show the direction of the shape anisotropy of the free magnetic layers of the bits; the arrows inside the ellipses indicate the orientations of the free-layer magnetization.

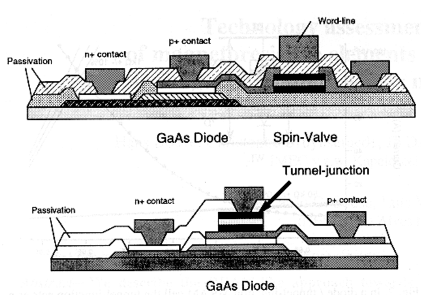


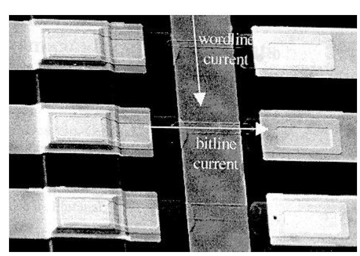


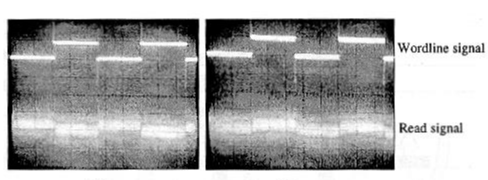
IBM J R&D, 2006

Spin valve

A 1D/1R SV cell







Pseudo spin valve

Introduction

Pseudo spin valve (PSV)
- Basic structure and operation method
- Performance of a PSV unit
  - Effect of word line pulse width

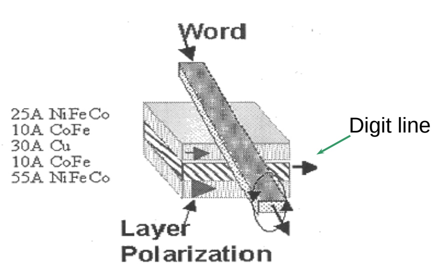
Pseudo spin valve

Basic structure

Concept: Direction of magnetization can be switched in both FM layers, but at **different** strength of the external field ➔ "soft" and "hard" layers.

Spacer is conductive.

The hard layer is used for information storage ➔ "0“ / "1”

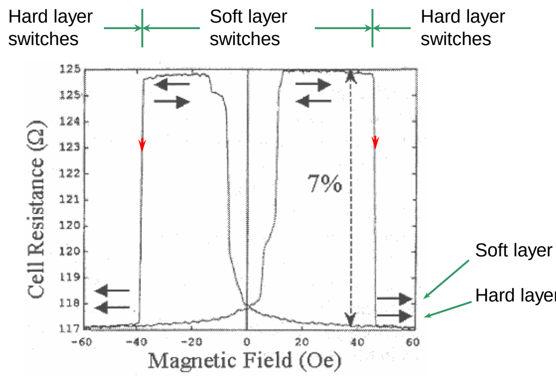


Pseudo spin valve

Operation of a PSV unit

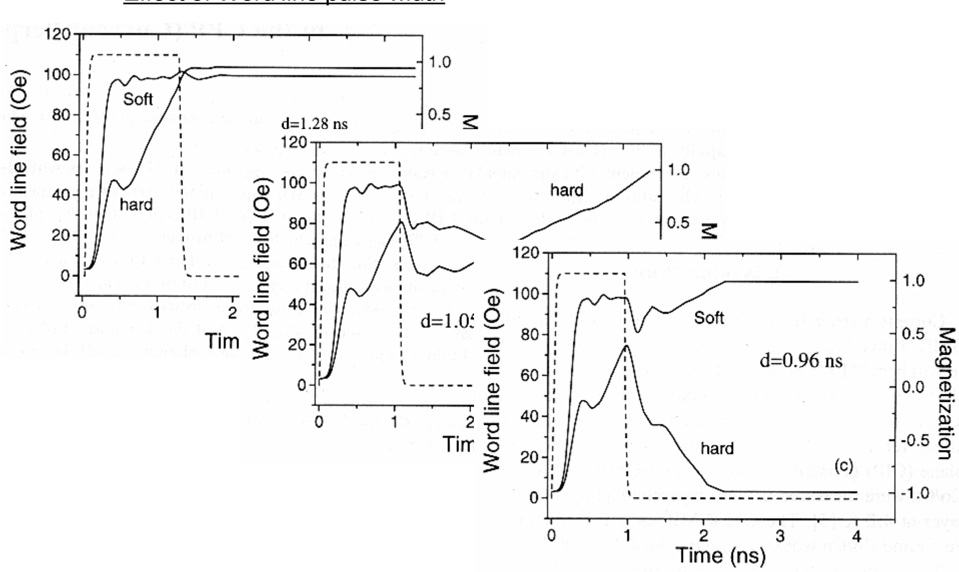
Read-out is achieved by detecting the MR changes during switching the soft layer while the hard layer remains unchanged.

Storing four states (2 bits) per cell is possible.



Pseudo spin valve

Effect of Word line pulse width



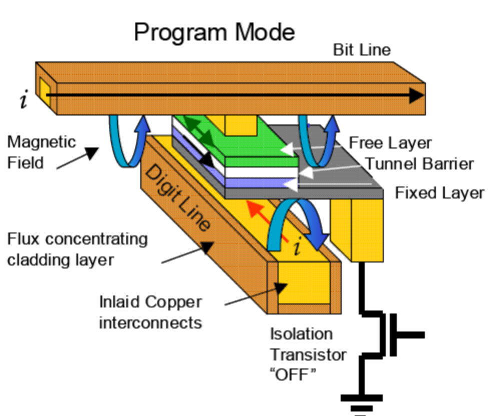
Magnetic tunnelling junction

Introduction

Magnetic tunnelling junction (MTJ)
- – Basic structure
- – MTJ cell and array
- – Performance of an MTJ unit
    - Temperature dependence
    - Effect of the MTJ spacer thickness
    - Different aspect ratios of the junction area

Magnetic tunnelling junction

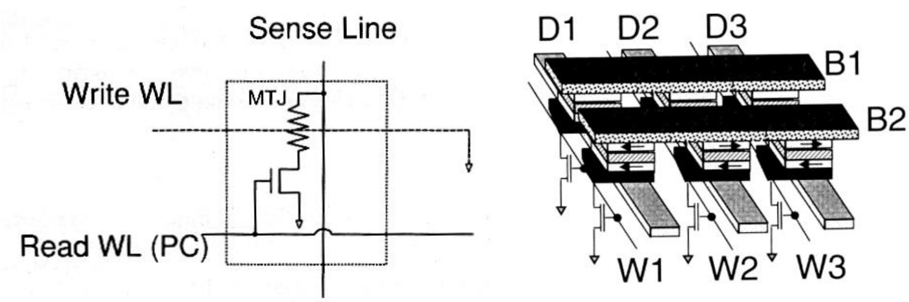
Basic structure



- Similar arrangement as a SV in CPP configuration, but the spacer is made of insulator and acts as a tunnelling barrier.
- Isolation transistor:
  READ: ON
  WRITE: OFF
- Motorola's flux concentrating cladding layer to reduce the WRITE power consumption.

Magnetic tunnelling junction

MTJ cell and array



Magnetic tunnelling junction

Operation of an MTJ unit

Read operation similar to PSV. 2bit/cell is also possible.

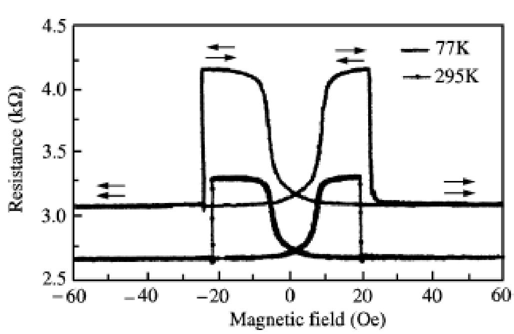
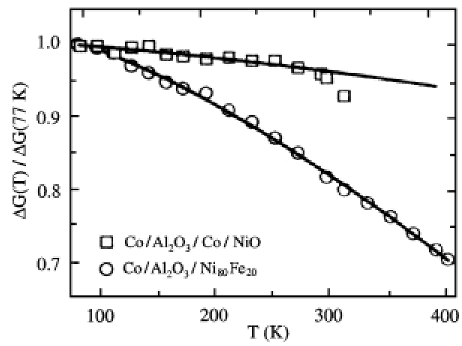


Fig. 3. Resistance versus applied magnetic field for a $Co/Al_2O_3/Ni_{80}Fe_{20}$ junction at room temperature and 77 K, showing JMR values of 20.2 and 27.1%, respectively. The barrier is formed by oxidation of a 8 Å Al layer (after Ref. [23]).

Magnetic tunnelling junction

Some issues – Temperature dependence



Magnetic tunnelling junction

Some issues – Effect of spacer thickness

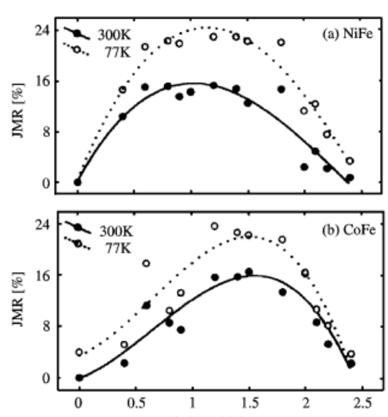


Fig. 4. Junction magnetoresistance plotted as a function of the thickness of the Al metal overlayer used to form the Al_2O_3 barrier in (a) $Co/Al_2O_3/Ni_{80}Fe_{20}$ and (b) $Co/Al_2O_3/Co_{50}Fe_{50}$ tunnel junctions (after Ref. [34]).

Magnetic tunnelling junction

Some issues – Aspect ratio of junction area

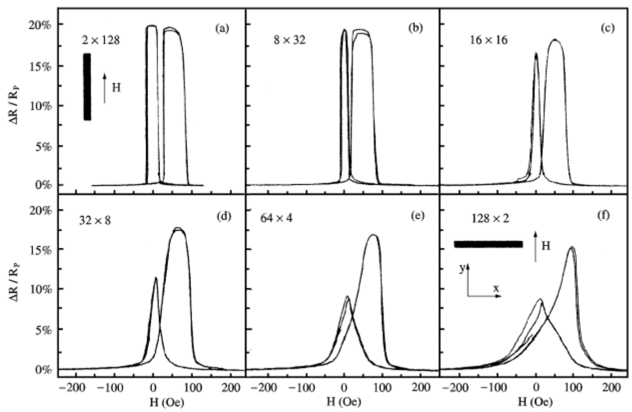


Fig. 6. Magnetoresistance curves at room temperature for a series of junctions with an identical area (256 μm^2) but having different aspect ratio (after Ref. [31]).

MRAM summary

Some relevant topics

Comments and challenges

Motorola MRAM demonstrator

Performance comparison of some NVMs

MRAM summary

Comments and challenges for MRAM

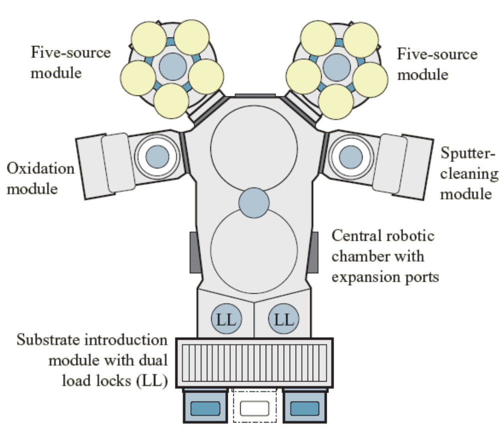
CPP vs CIP ➔ Vertical structure good for scale down to small size.
SV vs MTJ ➔ Higher resistance for faster speed.

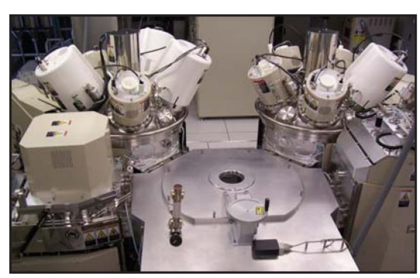
Metal contamination ➔ Ta layers both sides.
Metal inter diffusion within the sandwich structure at the temperature of Al/Cu interconnect process.
Power consumption of WRITE operation.
Reliable magnetic switching.
Uniformity of the very thin spacer (2-3nm) for 8-12 in wafers.

…

MRAM summary

A deposition system for MTJ



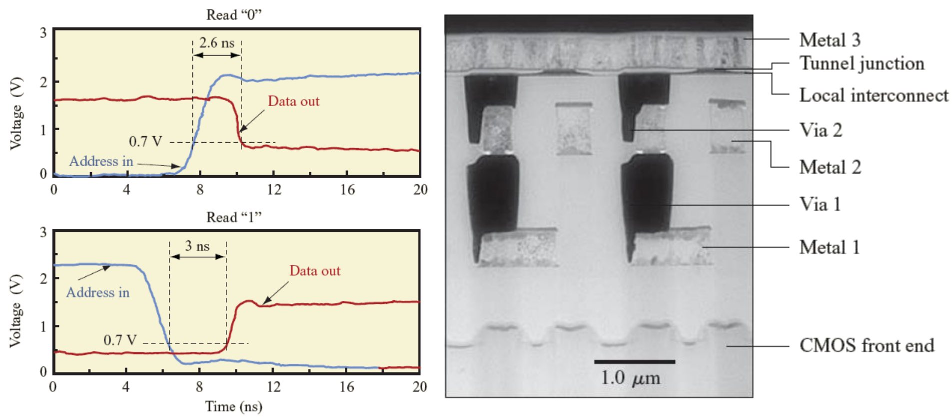


A system installed at IBM suitable for fabricating MTJs on 200-mm or 300-mm diameter wafers, showing part of central robotic chamber in the foreground, two five-source modules in the background (left and right), and a cleaning (etching) module at the lower left.

Canon ANELVA

MRAM summary

IBM CMOS MRAM: 1Kb FET twin cell

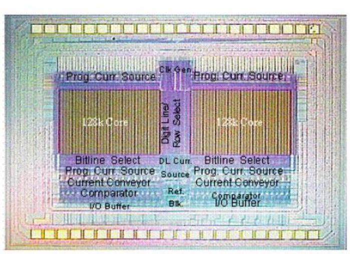


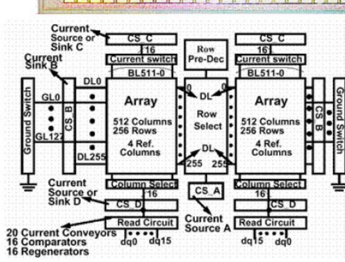
The first CMOS MRAM array fabricated at IBM — a 1Kb array containing FET twin cells fabricated in a 0.25μm technology: Time traces of input and output signals during read access operation and SEM cross section of twin-cell structure.

IBM, VLSI TSA TECH, 2005

MRAM summary

Motorola 256Kb MRAM





Feb. 2001 / June 2002

Features:

- 256 kB / 1 MB
- on 200 mm Si wafer
- 2x128k blocks / 16x64k blocks
- 1MTJ/1Tr
- reference cells
- five-layer metallization / magnetic cladding
- chip size: 3.9x3.2 mm² (40% for memory)
- write current: 11 mA / 3 mA

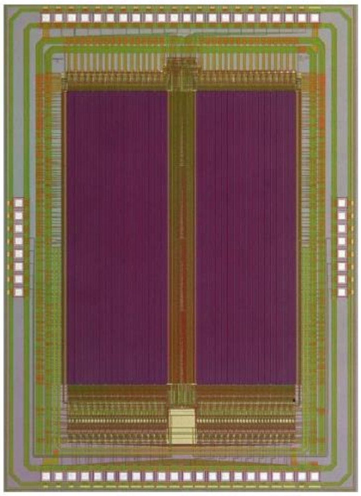
Wafer uniformity for 0.6x1.2 μm² cells:

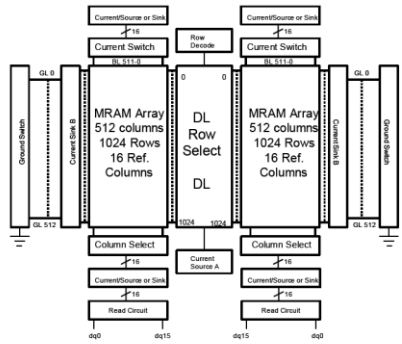
- TMR = 44.6 ± 0.7 %
- R_A = 9.97 ± 0.43 kΩμm²

from H. Brückl, Oct 2003

MRAM summary

Motorola 1Mb MRAM



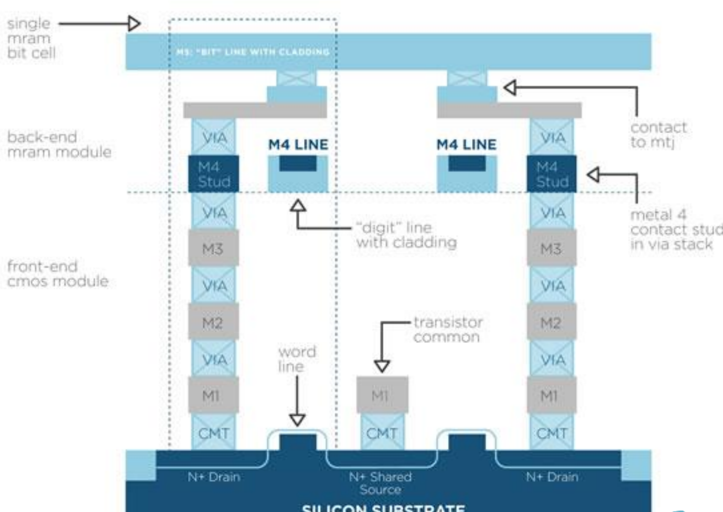


1T/1MTJ with Cu interconnects

Motorola, VLSI 2002

MRAM summary

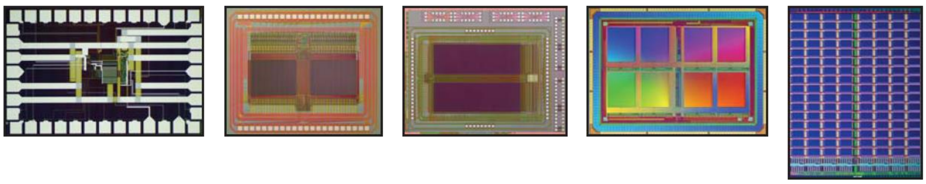
Everspin (Motorola) embedded process



EVERSPIN *2009*

MRAM summary

Increasing density of prototype MRAM chips (not to scale)



(a) (b) (c) (d) (e)

(a) IBM 1mmx1.5mm 1Kb chip with a 5.4μm² twin cell in 0.25μm technology with approximately 3-10ns access time; ©2000 IEEE.
(b) Motorola 3.9mmx3.2mm 256Kb chip with 7.1μm² cell in 0.6μm technology with 35ns access time. ©2001 IEEE;
(c) Motorola 4.25mmx5.89mm 1Mb chip with 7.1μm² cell in 0.6μm technology with 50ns access time; ©2002 IEEE.
(d) Motorola 4.5mmx6.3mm 4Mb chip with 1.55μm² cell in 180nm technology with 25ns access time; ©2003 IEEE.
(e) IBM 7.9mmx10mm 16Mb chip with 1.42μm² cell in 180nm technology with 30ns access time; ©2004 IEEE.

… … 32Mb, 64Mb and 128Mb (NEC & Toshiba), 512Mb (IBM?)

MRAM summary

Status of MRAM development

Update: Jan'05	Toshiba / NEC	TSMC	Sony	Samsung	IBM/IFX	Renesas	Motorola
Technology generation	0.13 μm	0.18 μm	0.18 μm	0.24 μm	0.18 μm	0.13 μm	0.18 μm
Demonstrator density	1 Mbit	1 Kbit	1 Mbit	Only cells	16 Mbit	1 Mbit	4 Mbit
MRAM type	Cross Point	1T2UMTJ ExtVia	Saturn shaped MTJ	MTJ + SAF			Toggling MRAM
Operation Voltage	1.5 V	1.8 V	1.1 V		1.8V (internal)	1.2 V	NA
Acces time	250 nsec	40 nsec	NA		30 nsec	5-10 nsec	25-35nsec
Write current	4 mA	4.5 mA	NA			> 3mA	NA
Cell size (1T1C)	NA	1.06 μm²	2.07 μm²		1.42 μm²	0.81 μm²	0.54 μm²
	6 F²	33 F²	64 F²	8 F²	44 F²	48 F²	16.7 F²
Comments	-	Scalable to 6 F²	-		3 masks	-	"product"
Source	IEDM '04	IEDM '04	VLSI '04	VLSI'04 / IEDM'03	VLSI /'04	IEDM '04/ VLSI '04	IEDM'03

D Wouters, IMEC

NVM comparison and reflection

Parameter	DRAM	SRAM	NOR Flash	NAND Flash	FeRAM	MRAM
Read cycles	$>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$ before cycling	10^{12}–10^{15}	$>10^{15}$
Write cycles	$>10^{15}$	$>10^{15}$	10^4–10^5	10^6	10^{12}–10^{15}	$>10^{15}$
Write voltage (V)	2.5–5	3.3–5	10/−10	18	0.8–5	0.8–5
Cell write time (ns)	10–100	1–50	6×10^3	2×10^5	10–50	10
Write energy (pJ)	Few 10^{-2}		9000	1	1	10–100
Random access time (ns)	40–70	6–70	150	~10 000	40–70	40–70
Cell size (F^2)	8	~100	12	4.6	9–13	6–10
Retention (years)	None	None	10	10	10	10
Scaling issues	Charge		Tunnel oxide → read current → access time	Erase voltage tunnel oxide scaling, SILC	3D + material texture	Switching field increase with scaling and uniformity
Status/forecast	256 Mb/1 Gb	4–16 Mb	32 Mb/128 Mb	256 Mb/1 Gb	1 Mb/4 Mb	few kb/1 Mb by 2002(?)
Applications	PC memory	Cache memory	Program code & data	Data files (camera, MP3)	Contactless smartcard	Envisaged: embedded (SOC) and mass storage

J D Boeck, et al, Semicond. Sci. Technol. 17, 342 (2002)

NVM comparison and reflection

Technology	Memory Mechanism	Fundamental Particle	Particles in a 20nm Cell	Comment
DRAM	Electrons stored on a capacitor	electron	~100,000	25fF*0.6V
NAND	Electrons stored on a floating gate	electron	~50/state	
Phase Change	Crystalline state Amorphous State	Atomic Bond, Bond Angle Bond configuration Ge octahedral/tetragonal coordination	~5E4	
RRAM	Conducting Filament Broken Filament	Cu ion or oxygen vacancy	few hundred	Constant with scaling
STRAM	Correlated electron spins (Bohr Magnetons)	Bohr Magneton	~40,000	20nm diameter X 2nm thick free layer 2 μ_B / Co, Fe atom
Ferro Electric DRAM	Correlated dipoles	Ferroelectric Dipole	~700,000	Capacitor matched to DRAM at 20μC/cm²

K Prall, et al, Micron, 2013

NVM comparison and reflection

Technology	State change	Barrier between states	Method of modifying barrier
DRAM	Electrons stored in a dielectric	Energy required for electrons to leak through p-n junction of MOS transistor	Turning transistor on/off
NAND	Electrons stored in the floating gate	Energy required to tunnel through tunnel oxide barrier/IPD	Electric Field induced Fowler-Nordheim Tunneling
Ferroelectric	Energetically Bi-stable states Ferroelectric domain polarity	Energy required to switch polarity	Electric field overcoming ferroelectric polarity
Phase Change	Energetically Bi-stable states Crystallinity of the material	Energy required to switch crystallinity	Thermal Energy
RRAM	Ions stored in a dielectric	Energy required to ionize and migrate metal or oxygen ions	Electric field driven ionic conduction
STRAM	Energetically Bi-stable states Magnetic Anisotropy of free layers	Energy required to switch polarity	Spin Torque

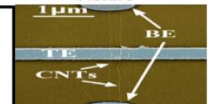
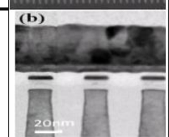
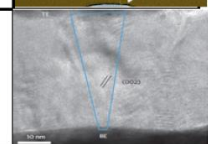
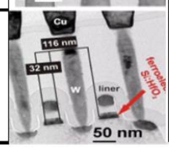
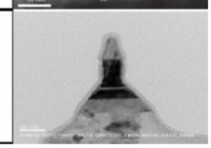
K Prall, et al, Micron, 2013

NVM comparison and reflection

Current or Field Based	Technology	Typical Input Energy 20nm cell	Input Energy 20nm Cell (J)	Energy Efficiency = Energy Retained/Energy Input	How is Energy Corresponding to Retention Loss Calculated	Primary Write State Loss Mechanism
Field	DRAM	$E=1/2\ CV^2$ $=1/2 * 25fF * 1.2^2$	1.80E-14	~1	Zero Loss	Relaxation, Dielectric leakage
Field	NAND	$E=1/2\ CV^2$	1.00E-16	~1	Zero Loss	Electrons trapped outside of floating gate
Field	Ferroelectric	Integrate V(t)I(t) 25 uC/sq. cm 0.5 u^2 capacitor area	3.00E-13	~0.8-1	~Zero Loss	Only edge dipoles contain a usable signal, Center dipoles compensated. Final vs. remnant polarization
Current	NOR	E=I*V*τ	~1E-9 (50nm cell)	~1E-6	$E=1/2\ CV^2$	Very few lucky electrons injected on the floating gate
Current	Phase Change	E=I*V*τ =100uA * 2.5V * 250nS	6.25E-11	~4.4E-5/1.4E-6	Phase transition barrier (Amorphous -> Crystalline 2.3eV 5nm)	Thermal energy loss outside of chalcogenide
Current	RRAM	E=I*V*τ =50uA * 2.5V * 50nS	6.25E-12	~ 2E-3/1.2E-4	Activation barrier for charged vacancy diffusion (0.5eV) in HfOx (post formation)	Thermal energy loss Parasitic current
Current	STRAM	E=I*V*τ =40uA * 0.4V * 10nS	1.6E-13	~1.5E-6	60KT/ Input Energy	Spin Related thermal agitation tunneling efficiency stochastic switching

K Prall, et al, Micron, 2013

NVM comparison and reflection

Technology	Demonstrated Scalability	Picture	Technology	Demonstrated Scalability	Picture
DRAM	<20nm		Phase Change [19]	~1nm	
NAND [17]	~15nm Planar Cell		RRAM [20]	~5nm Typical Filament size	
Ferroelectric [18]	~30nm FEFET		STRAM [21]	~20nm	

[17] N. Ramaswamy, et al., IMW 2013
[18] J. Muller, et al., VLSI 2012, pg. 26
[19] J. Liang, et al., IEEE TRED, Apr. 2012, pg. 1155
[20] D-H Kwon, et al., Nature Nanotechnology, Jan. 2010, pg. 148
[21] W. Kim, et. al., IEDM 2011, 24.1.2, pg. 532

K Prall, et al, Micron, 2013