UNIVERSITY OF CAMBRIDGE

Solid State Devices

4B6

Lecture 7/8 – FRAM

Daping Chu

Lent 2016

Memory device

Introduction

Random Access Memory
- RAM, DRAM and NV Memories
- Trends and limits

Some real FRAM devices
- Early stage
- Recent development

Memory device

RAM

RAM – Random Access Memory:

Time to access a datum (nearly) *independent* of where the information (bit – binary digit) is physically stored.

Different from sequential devices:

tape drives, floppy/hard disks, …

Two types of RAMs in every day life

– SRAM: Static RAM – fast, stable, 4T-6T

– DRAM: Dynamic RAM – slower, unstable, 1T

Memory device

Non-volatile memory

NV (Non-volatile) Memory

– Information kept after power off

– EEPROM, Flash Memory, FRAM, MRAM, …

Applications

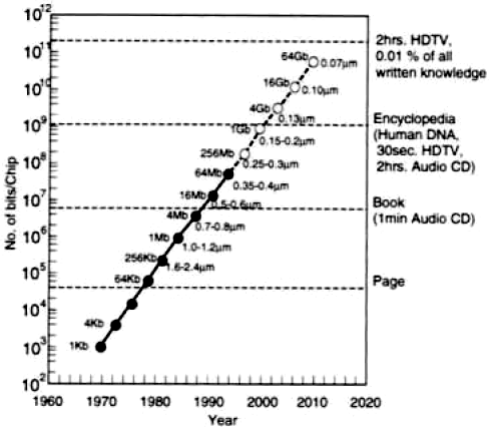
– Stand alone memory chips

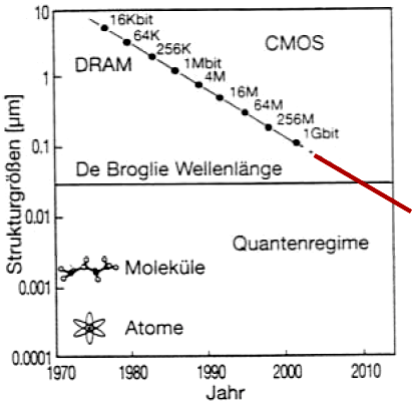
To replace stand alone DRAMs and SRAMs

– Embedded memories (e.g. system-on-chip)

Memory device

Trends and limits



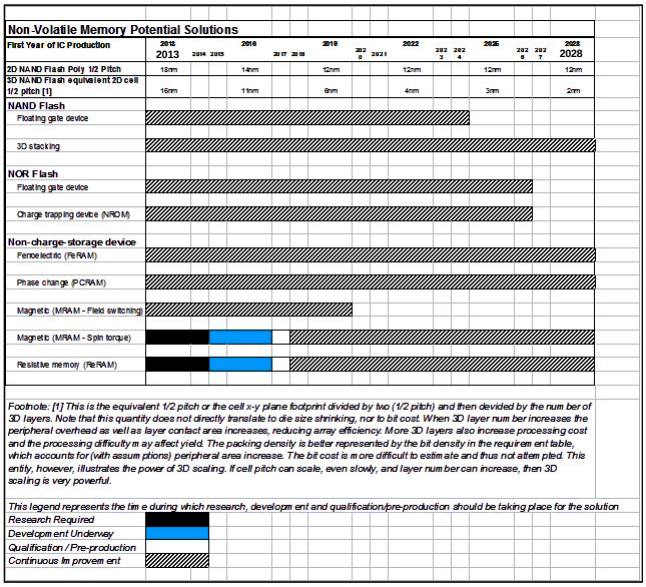


International Technology Roadmap for Semiconductors (ITRS)

First published as National Technology Roadmap of Semiconductors by Semiconductor Industry Association (SIA) in 1993:

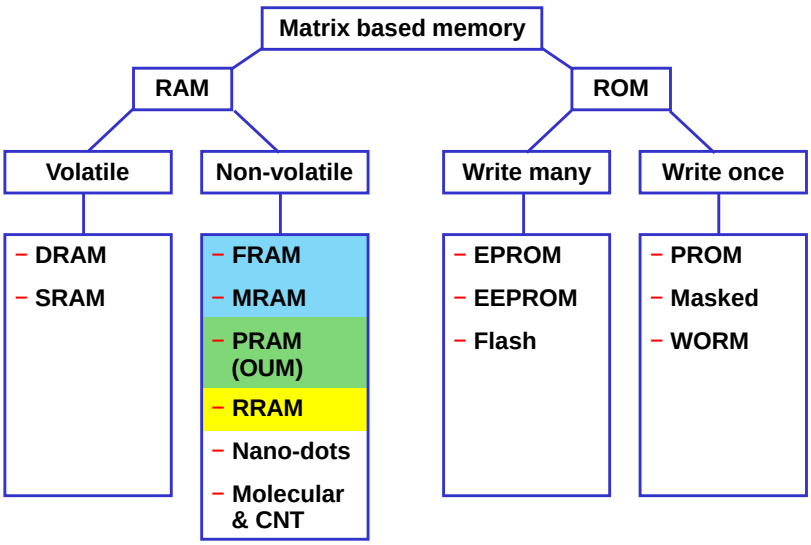
Characteristic	1992	1995	1998	2001	2004	2007
Feature size (microns)	0.50	0.35	0.25	0,18	0,12	0.10
Gates per chip (millions)	0.3	0.8	2.0	5.0	10.0	20.0
Bits per chip						
DRAM	16M	64M	256M	1G	4G	16G
SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm²)	$4.00	3.90	3.80	3.70	3.60	3.50
Chip size (mm²)						
logic	250	400	600	800	1,000	1,250
memory	132	200	320	500	700	1,000
Wafer diameter (mm)	200	200	200-400	200-400	200-400	200-400
Defect density (defects/cm²)	0.10	0.05	0.03	0.01	0.004	0.002
Levels of interconnect (for logic)	3	4-5	5	5-6	6	6-7
Maximum power (watts/die)						
high performance	10	15	30	40	40-120	40-200
portable	3	4	4	4	4	4
Power supply voltage						
desktop	5	3.3	2.2	2.2	1.5	1.5
portable	3.3	2.2	2.2	1.5	1.5	1.5

ITRS 2013 for NVM 2013-2028

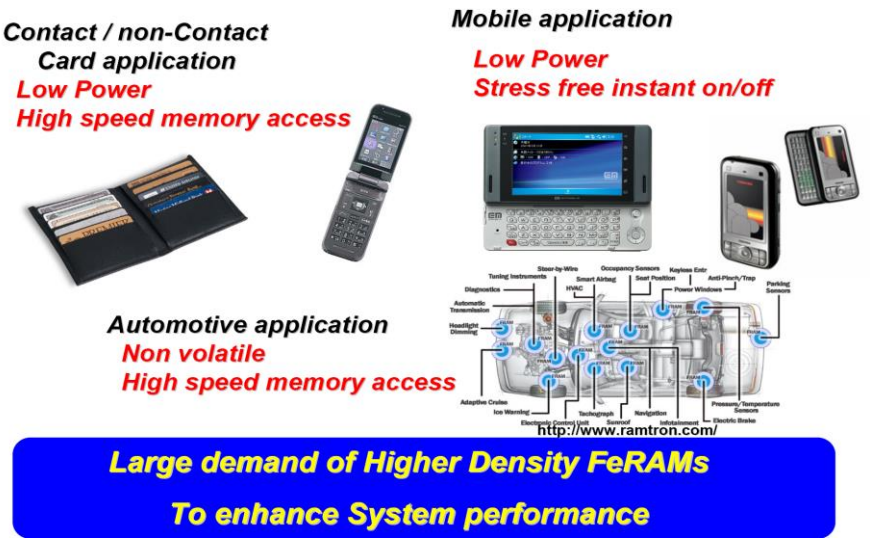


Memory device

Memory classification

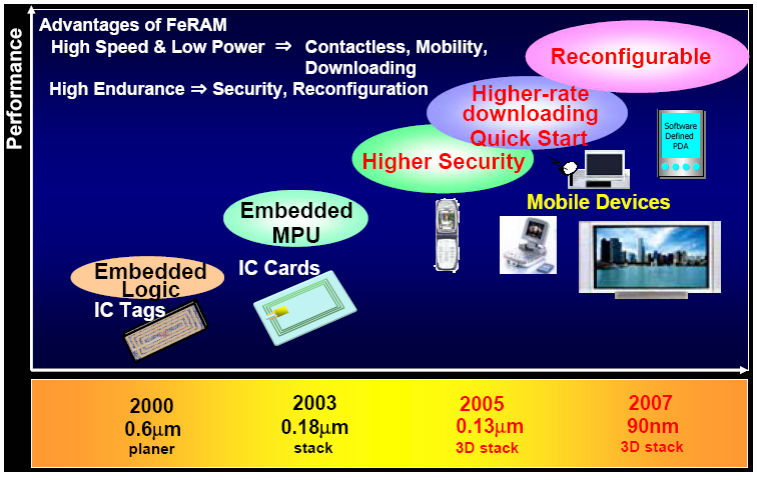


FRAM – devices



Toshiba, 2007

FRAM – devices

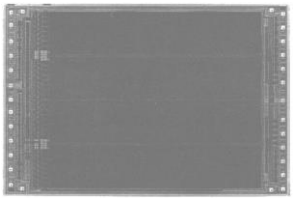


Panasonic, 2003

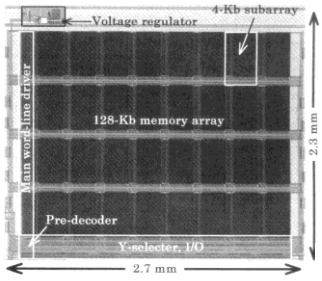
In January 2008, Japanese Railway announced all across Japan, the standard JR E-Tickets, E-Purses and credit cards are to use FRAM card (Panasonic 0.18μm).

FRAM – devices

Early examples

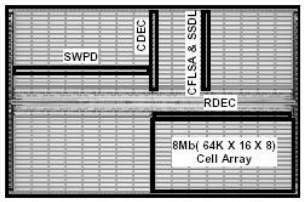


A 256kb FRAM, which consists of four 64Kb arrays. Peripheral circuits locate at the left and right sides of the chip.
(1T/1C, Y1, Matsushita, 1995)



Technology	0.35um 3-metal CMOS, CMVP proces
Organization	32-Kb, 64-Kb, 128-Kb, 8-I/O
Cell size	18.7 μm² (2T/2C)
Chip size	6 mm² (128-Kb)
Supply Voltage	2.7 V to 5.5 V
Active Current	0.3 mA (2.5 MHz, 2.7 V)

A 128Kb FRAM array.
(2T/2C, SBT, NEC, 2000)

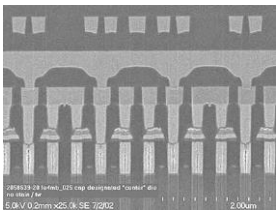


Density	32M
FRAM Technology	0.25μm
Chip Size	12420μm x 7268 μm = 90.2mm²
Configuration	1T/1C, COB
Cell Size	0.7728μm x 1.2144μm = 0.9384μm²
Cap Size	0.4784μm x 0.92μm = 0.44μm²
Operation Voltage	2.7V~3.3V
Address Access Time	50 nsec
Stand-by Current	<10μA

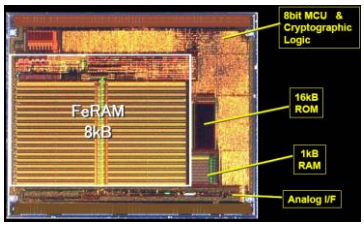
A 32 Mb FRAM array.
(1T/1C, PZT, Samsung, 2002)

FRAM – devices

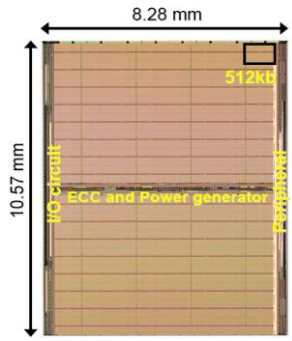
Recent development



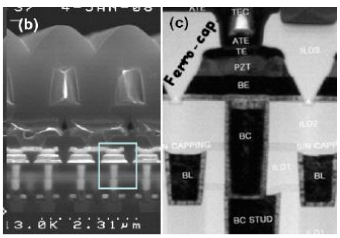
Texas Instrument, 2003
64Mb, 0.25μm, PZT
(0.09μm in progress)



Panasonic, 2003
8Kb, 0.18μm, SBT, SoC (Embedded)



Toshiba, 2007
64Mb, 0.13μm, PZT
Chain memory



Samsung, 2008
64Mb, 0.18μm, PZT

Ferroelectrics

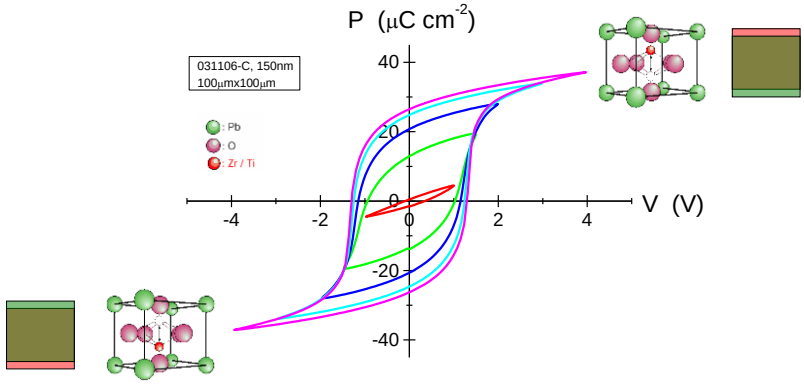
Materials

Material behaviours
– Polarization and domains
– Characterization – hysteresis

Lead Ziconate Titanate (PZT)
– Microscopic vs Macroscopic

Ferroelectrics

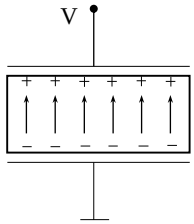
$PbZr_{1-x}Ti_xO3$ (PZT)

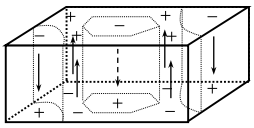


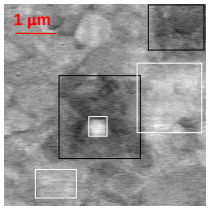
Bi-stable states ⇔ 1 bit (“0” or “1”)

Ferroelectrics

Polarisation domain

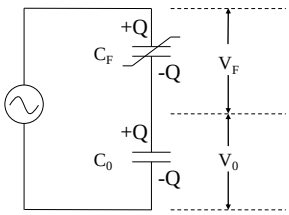




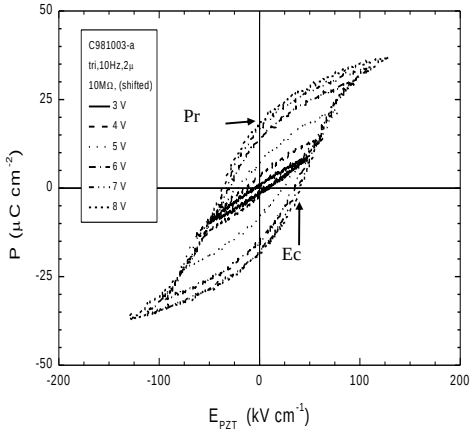


Ferroelectrics

Polarisation domain



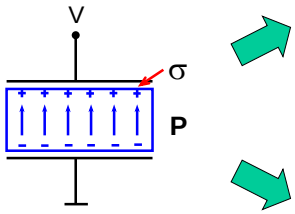
Sawyer-Tower method



Pr – Remnant polarization
Ec – Coercive field

FRAM – memory cell

Charge vs Field



- Charge approach

$$\Delta Q = A\,\Delta P$$

- Field approach

$$E \propto P$$

FRAM – memory cell

Two approaches for Read-Out

Charge approach

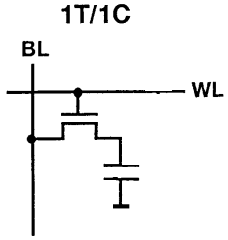
- F-cap ➔ 1T/1C cell, …
- WRITE and READ
- Structure and Fabrication Process

Field approach

- FFET
- Cell, Structure and Operation

FRAM – memory cell

A DRAM cell



Read:

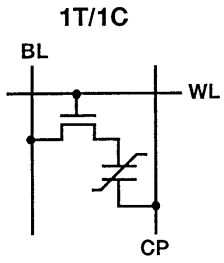
Drive Word Line (WL)
Sense value on Bit Line (BL)
(saved value destroyed)

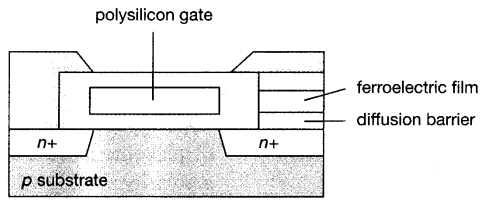
Write:

Drive WL
Drive new value on BL

FRAM – memory cell

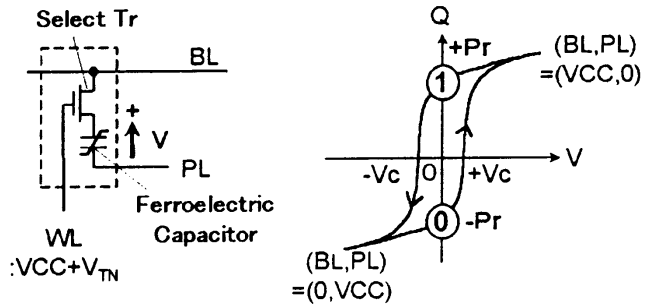
A 1T/1C FRAM cell – configuration





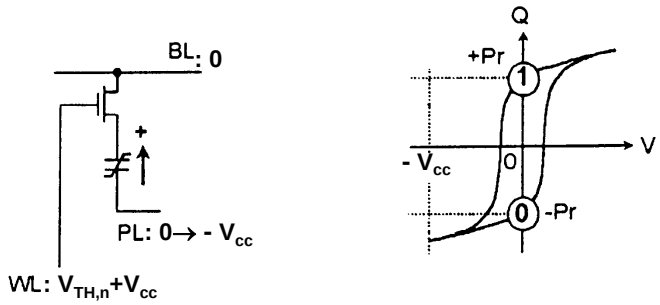
FRAM – memory cell

A 1T/1C FRAM cell – WRITE operation



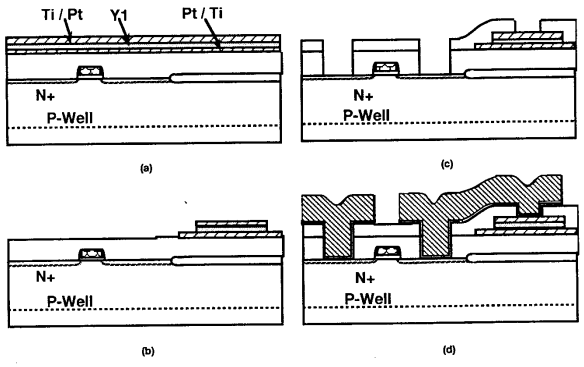
FRAM – memory cell

A 1T/1C FRAM cell – READ operation



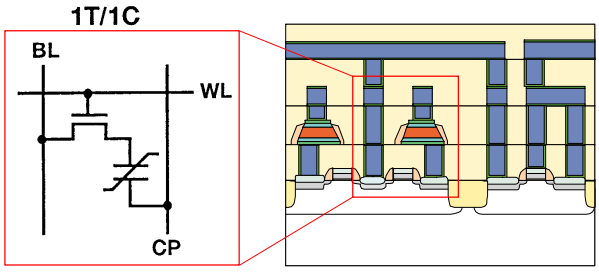
FRAM – memory cell

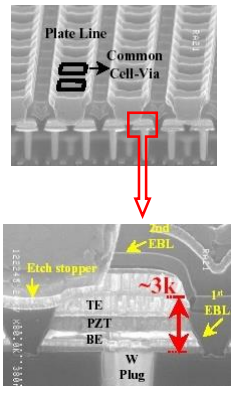
Fabrication process



FRAM – memory cell

Stacked architecture

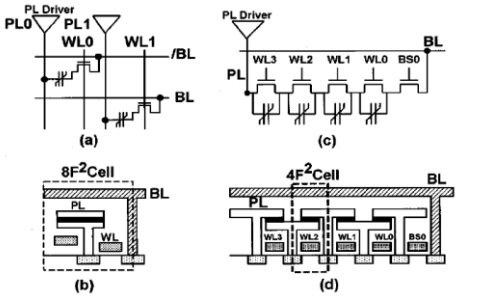


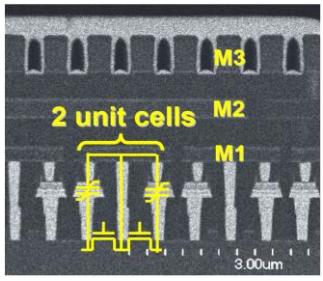


32Mb, 0.25μm
Samsung, 2002

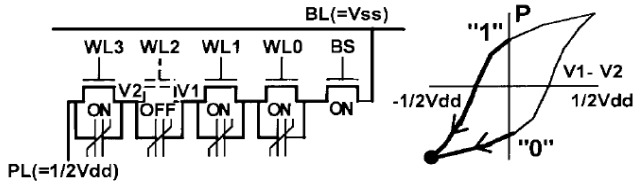
FRAM – memory cell

Chain memory



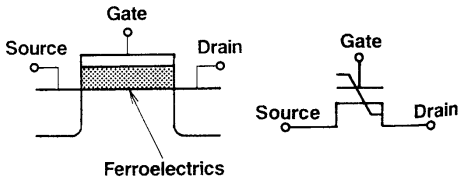


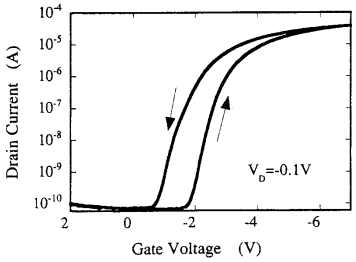
Kunishima, Toshiba, 2007

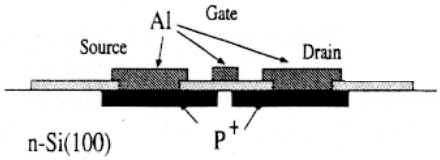


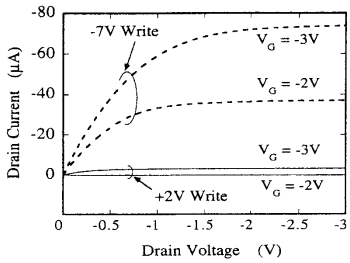
FRAM – memory cell

Ferroelectric FET



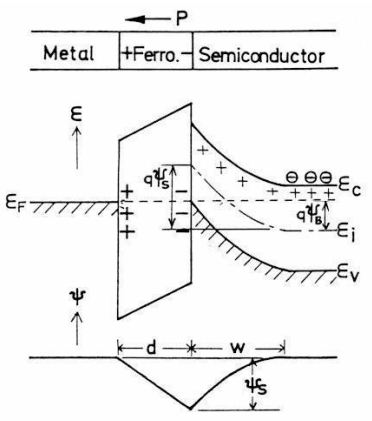






FRAM – memory cell

Ferroelectric FET



The threshold voltage, V_{TH} , is:

$$V_{TH} = V_{FB} + 2\psi_B + V_B$$
$$= \left(\phi_{MS} - \frac{\sigma_i + \sigma_P}{c_F} \right) + 2\psi_B + V_B$$

where ϕ_{MS} - the metal-semiconductor work function difference;

V_B - the effective bulk charge voltage;
(For p-type bulk: $V_B = (4qN_A\varepsilon_s\varepsilon_0\psi_B)^{1/2} / c_F$)

σ_i - the surface charge density at the interface between ferroelectrics and semiconductor;

σ_P - the effective polarization charge density of the ferroelectrics;

c_F - the ferroelectric capacitance per unit area.

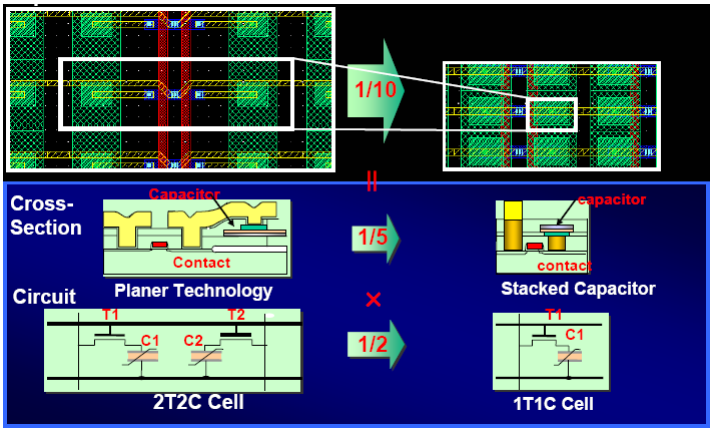
FRAM – some related issues

Challenges

Issues	Technical	Fundamental
• Scaling down	• Stacked capacitor • 3D • FFET	• Increase P_r • Interface states
• Reliability	• Hydrogen proof	• Fatigue free • Imprint • Retention
• Low voltage operation	• Thinner films	• Lower E_c • Low leakage

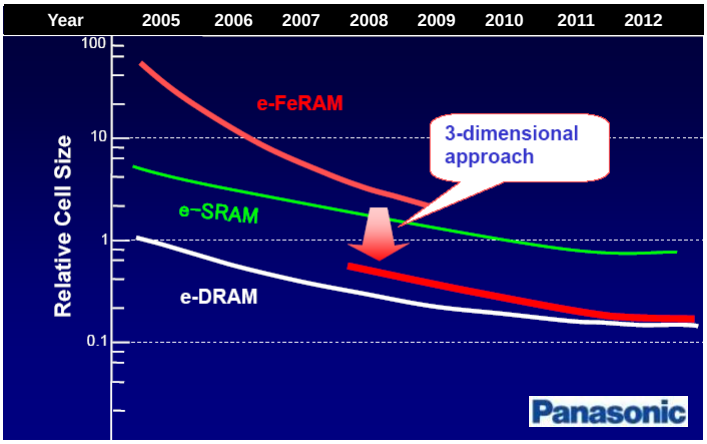
FRAM – some related issues

Stacked capacitor



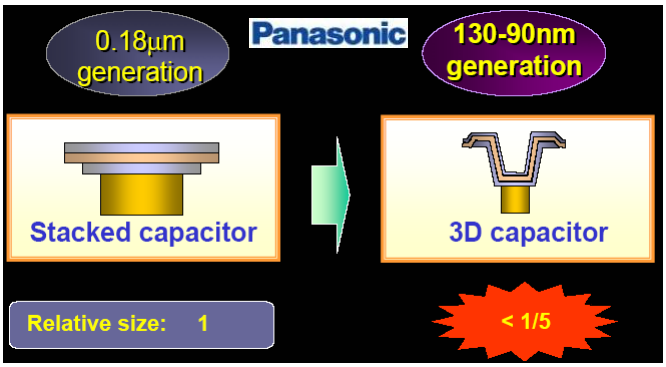
FRAM – some related issues

FRAM scaling



FRAM – some related issues

3D capacitor



TI: 3D when <90nm

FRAM – some related issues

Fundamental size limit?

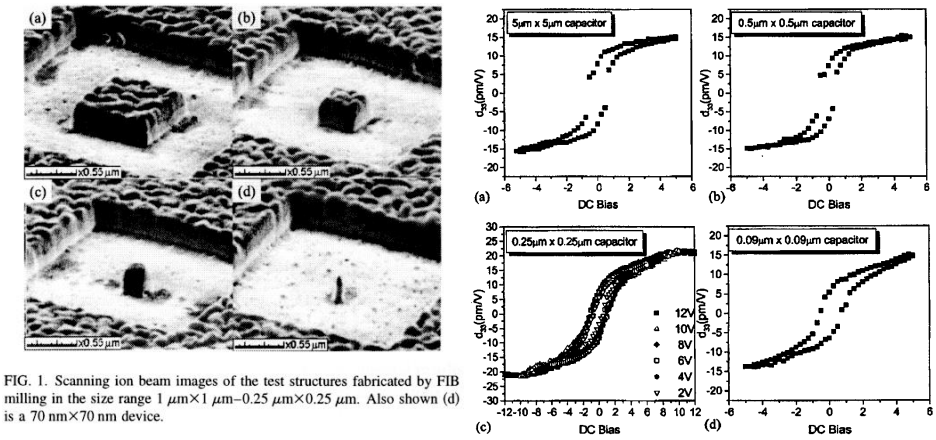
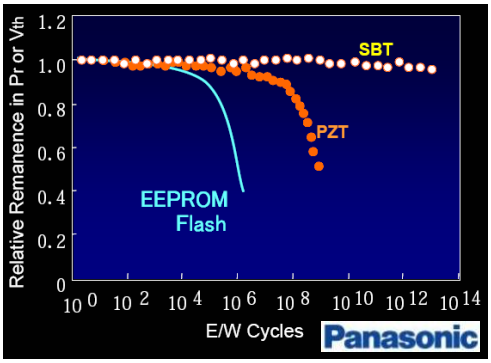


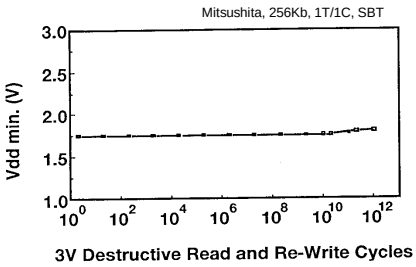
FIG. 1. Scanning ion beam images of the test structures fabricated by FIB milling in the size range 1 μm×1 μm–0.25 μm×0.25 μm. Also shown (d) is a 70 nm×70 nm device.

Operation down to 90nmx90nm checked.

FRAM – some related issues

Polarization fatigue

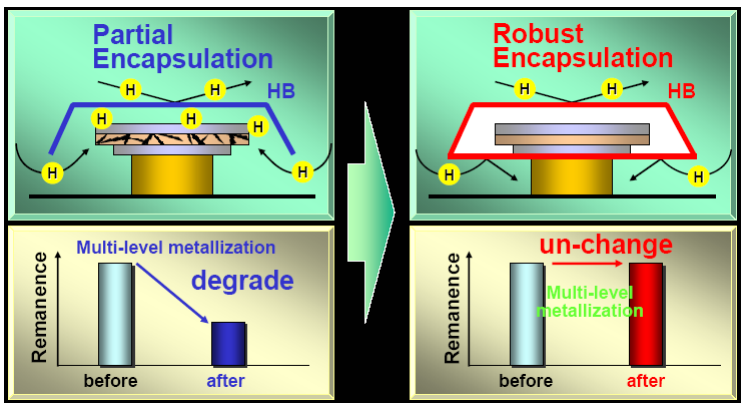




Now the switch endurance of FRAM cells with PZT can reach 10^{15} cycles.

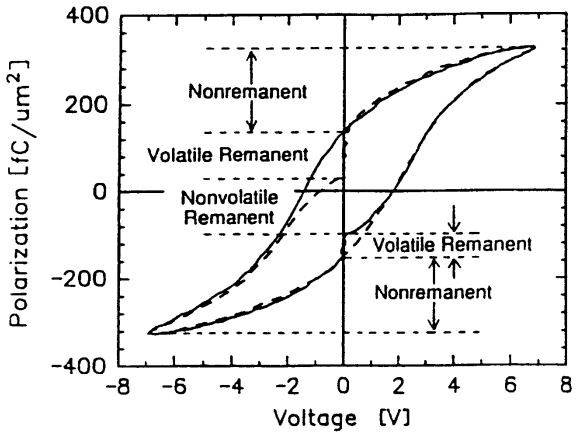
FRAM – some related issues

Enclosed hydrogen barrier



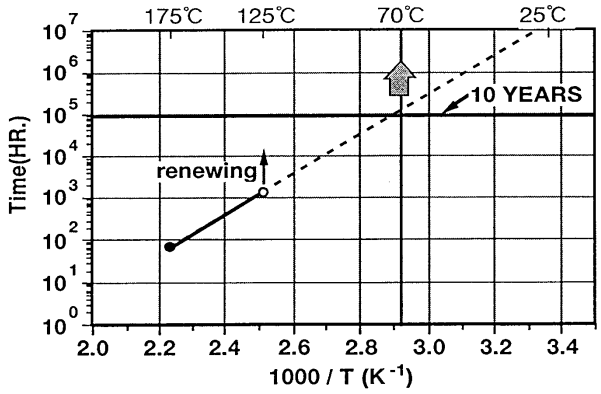
FRAM – some related issues

Retention



FRAM – some related issues

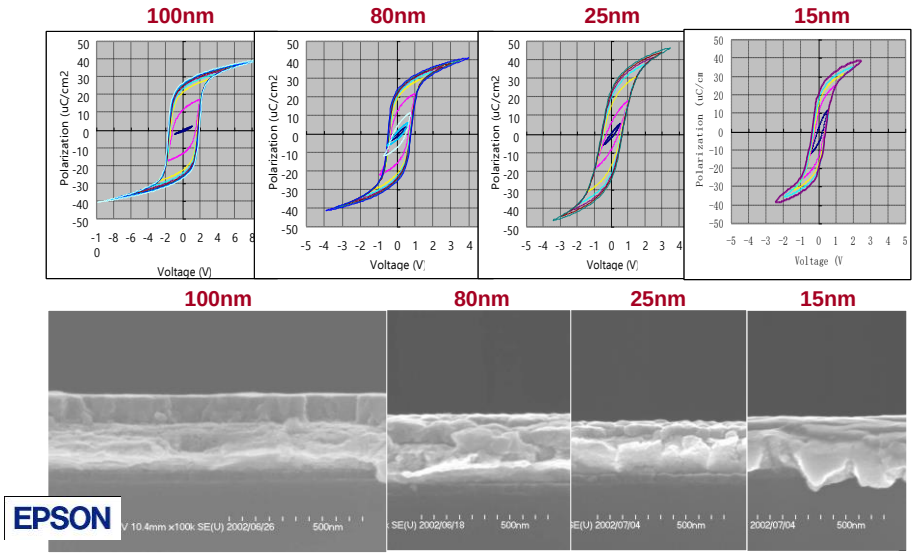
Failure time



Failure time vs temperature measured on a 256kb 1T/1C FRAM
➔ life time

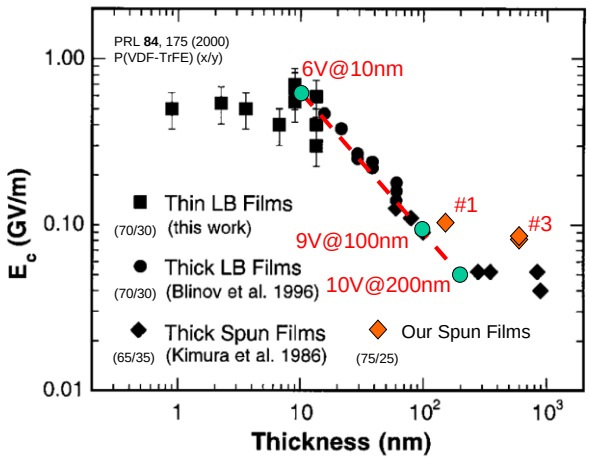
FRAM – some related issues

Thinner films



FRAM – some related issues

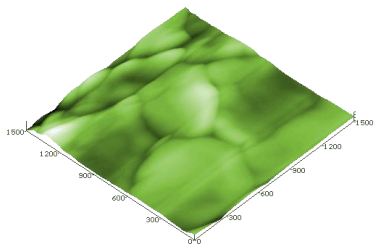
Possible restraint on low voltage operation



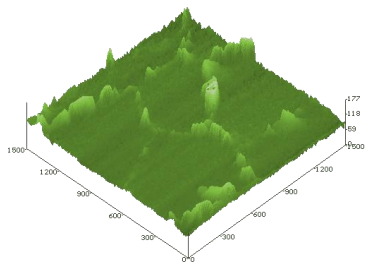
- It seems that decreasing the thickness of a P(VDF-TrFE) film from 100nm to 10nm only leads to a reduction of operating voltage from 9V to 6V!

FRAM – some related issues

Leakage current path



Topography



Leakage current

Leakage current along grain boundaries
(C9905-01, 60nm PZT on Ir)

FRAM – status and roadmap

Update: Jan '05	Hynix	Samsung		Toshiba	Matsushita		Fujitsu	Texas Inst Agilent Ramtron
Technology generation	0.25 µm	0.25 µm	0.18 µm	0.20 µm(?)	0.18 µm	0.18 µm	0.18 µm	0.13 µm
Demonstrator density	16 Mbit	32 Mbit	2Mb	64 Mbit	1 Mb	1 Mbit	4 Mbit	64 Mbit
Operation Voltage	3V	2.7-3.3V	1.6V	NA	1.5V (0.75V cell level)	1.1 V	1.8 V	1.3 V
Acces time	70 nsec	50 nsec		50 nsec	>250nsec	15 nsec	30 nsec	30 nsec
Cycle time	150 nsec		60 nsec	75 nsec	2 µsec			35nsec
Material	Sol-gel BLT	100nm Sol-gel PZT	100nm MOCVD PZT	(PVD) PZT	(MOD) SBTN	100nm MOD SBTN	120nm MOCVD PZT	MOCVD PZT
Cell size (1T1C)	1.5 µm²	0.9384 µm²	0.486 µm²	0.602 µm²	2.4 µm²	1.1 µm²	1.3 µm²	0.54 µm²
	24 F²	15 F²	15 F² (9F² poss)	15 F²	74 F²	34 F²	40 F²	32 F²
Cap size	0.71 µm²	0.44 µm²	0.261 µm²	0.25 µm²	NA	0.70 µm²	0.49 µm²	0.25 µm²
2.Pr	NA	38 µC/cm²	40 µC/cm²	NA	NA	18 µC/cm²	31 µC/cm²	24 µC/cm²
Active current/power	<20 mA	NA	25mA	NA	0.01mW	NA	16mA	16mA
STBY current	<10 µA	<10 µA	NA	NA	NA	NA	NA	NA
Source	ISIF '03 /IEDM'03	VLSI Tech '02 /'03	IEDM '04	VLSI Tech '04	VLSI Circuit '04	VLSI '03 (ISIF '03)	IEDM '02 / ISIF '03	VLSI '03 / IEDM '02

Highest density : 64Mb **Smallest cell size : 15 F2** **Lowest Voltage : 1.1V**
Fastest access : 15 nsec **Most advanced technology : 0.13µm, 5ML Cu/FSG**
Material : PZT (4), SBT(1), BLT (1)

D.Wouters IMEC

FRAM – status and roadmap

Year of Production	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
Logic Industry "Node Range" Labeling (nm) [based on 0.71x reduction per "Node Range" ("Node" = ~2x Mx)	"16/14"		"11/10"		"8/7"		"6/5"	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	40	32	32	28.3	25.3	22.5	20.0	17.9
DRAM ½ Pitch (nm) (contacted)	28	26	24	21	20	18	16	15
Planar (2D) NAND Flash uncontacted poly 1/2 Pitch (nm)	18	17	15	14	13	12	11	10
A. FeRAM (Ferroelectric RAM)								
Year of Production	2013	2014	2015	2016	2017	2018	2019	2020
FeRAM technology node – F (nm) [1]	130	130	130	90	90	90	90	90
MET1 1/2 Pitch - F/sm/(A)	175	175	175	135	135	135	135	135
FeRAM cell size – area factor a in multiples of F2 [2]	23	23	23	22	22	22	22	22
FeRAM cell size ($\mu m2$)	0.71	0.71	0.71	0.40	0.40	0.40	0.40	0.40
FeRAM cell structure [3]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
FeRAM capacitor structure [4]	stack	stack	stack	stack	stack	stack	stack	stack
FeRAM capacitor footprint ($\mu m2$) [5]	0.423	0.423	0.423	0.234	0.234	0.234	0.234	0.234
FeRAM capacitor active area ($\mu m2$) [6]	0.423	0.423	0.423	0.234	0.234	0.234	0.234	0.234
FeRAM cap active area/footprint ratio [7]	1	1	1	1	1	1	1	1
Ferro capacitor voltage (V) [8]	1.5	1.5	1.5	1.2	1.2	1.2	1.2	1.2
FeRAM minimum switching charge density ($\mu C/cm2$) [9]	8.5	8.5	8.5	12.0	12.0	12.0	12.0	12.0
FeRAM endurance (read/write cycles) [10]	1.00E+15	1.00E+15	1.00E+15	1.00E+15	1.00E+15	1.00E+15	1.00E+15	1.00E+15
FeRAM nonvolatile data retention (years)	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years
B. MRAM (Magnetic RAM)								
B1. Field switching MTJ MRAM[11]								
Year of Production	2013	2014	2015	2016	2017	2018	2019	2020
MRAM Technology Node F (nm)	90	90	65	65	65			
MRAM cell size area factor a in multiples of F2	51	51	52	52	52			
MRAM typical cell size (um2)	0.41	0.41	0.22	0.22	0.22			
MRAM switching field (Oe) [12]	67	67	82	82	82			
MRAM write energy (pJ/bit) [13]	120	120	110	110	110			
MRAM active area per cell (um2) [14]	0.124	0.124	0.066	0.066	0.066			
MRAM resistance-area product (Kohm-um2) [15]	1.2	1.2	0.6	0.6	0.6			
MRAM magnetoresistance ratio (%) [16]	65	65	90	90	90			
MRAM nonvolatile data retention (years)	>10	>10	>10	>10	>10			
MRAM write endurance (read/write cycles)	>3E16	>3E16	>3E16	>3E16	>3E16			
MRAM endurance – tunnel junction reliability (years at bias) [17]	>10	>10	>10	>10	>10			
B2. Spin-Torque Transfer (STT) MRAM								
Year of Production	2013	2014	2015	2016	2017	2018	2019	2020
MRAM technology node F (nm) [18]	90	90	65	65	45	45	45	32
MRAM cell size area factor a in multiples of F2	28	28	20	20	15	14	14	10
MRAM typical cell size (um2)	0.23	0.23	0.08	0.08	0.030	0.028	0.028	0.010
MRAM materials technology (In -plane Magnetic Anisotropy (IMA) or Perpendicular Magnetic Anisotropy (PMA))	IMA	IMA	IMA	IMA	PMA	PMA	PMA	PMA
MRAM switching current (uA) [19]	340	310	200	175	120	120	100	50
MRAM write energy (pJ/bit) [20]	4.3	3.9	2.5	2.5	1.2	1.2	1	0.3
MRAM active area per cell (um2) [21]	0.021	0.019	0.01	0.008	0.006	0.006	0.005	0.004
MRAM resistance-area product (Ohm-um2) [22]	13.5	13.5	12.5	11	10	10	10	10
MRAM magnetoresistance ratio (%) [23]	120	120	120	120	150	150	150	150
MRAM nonvolatile data retention (years) [24]	>10	>10	>10	>10	>10	>10	>10	>10
MRAM write endurance (read/write cycles) [25]	>1E12	>1E12	>1E12	>1E12	>1E12	>1E12	>1E12	>1E15
MRAM endurance-tunnel junction reliability (years at bias)	>10	>10	>10	>10	>10	>10	>10	>10

ITRS 2013

FRAM – status and roadmap

Year of Production	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*	*2028*
Logic Industry "Node Range" Labeling (nm) [based on 0.71x reduction per "Node Range" ("Node" = ~2x Mx)	"4/3"		"3/2.5"		"2/1.5"		"1/0.75"	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	15.9	14.2	12.6	11.3	10.0	8.9	8	7.1
DRAM ½ Pitch (nm) (contacted)	14	13	12	11	10	9	8	7
Planar (2D) NAND Flash uncontacted poly 1/2 Pitch (nm)	9	8	8	8	8	8	8	8
A. FeRAM (Ferroelectric RAM)								
Year of Production	2021	2022	2023	2024	2025	2026	2027	2028
FeRAM technology node – F (nm) [1]	65	65	65	65	45	45	45	45
MET1 1/2 Pitch - F/sm/(A)	105	105	105	105	80	80	80	80
FeRAM cell size – area factor a in multiples of F2 [2]	20	20	20	20	19	19	19	19
FeRAM cell size ($\mu m2$)	0.22	0.22	0.22	0.22	0.12	0.12	0.12	0.12
FeRAM cell structure [3]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
FeRAM capacitor structure [4]	stack	stack	stack	stack	stack	stack	stack	stack
FeRAM capacitor footprint ($\mu m2$) [5]	0.125	0.125	0.125	0.125	0.067	0.067	0.067	0.067
FeRAM capacitor active area ($\mu m2$) [6]	0.125	0.125	0.125	0.125	0.067	0.067	0.067	0.067
FeRAM cap active area/footprint ratio [7]	1	1	1	1	1	1	1	1
Ferro capacitor voltage (V) [8]	1	1	1	1	1	1	1	1
FeRAM minimum switching charge density ($\mu C/cm2$) [9]	18.1	18.1	18.1	18.1	26.5	26.5	26.5	26.5
FeRAM endurance (read/write cycles) [10]	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16
FeRAM nonvolatile data retention (years)	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years
B. MRAM (Magnetic RAM)								
B1. Field switching MTJ MRAM[11]								
Year of Production	2021	2022	2023	2024	2025	2026	2027	2028
MRAM Technology Node F (nm)								
MRAM cell size area factor a in multiples of F2								
MRAM typical cell size (um2)								
MRAM switching field (Oe) [12]								
MRAM write energy (pJ/bit) [13]								
MRAM active area per cell (um2) [14]								
MRAM resistance-area product (Kohm-um2) [15]								
MRAM magnetoresistance ratio (%) [16]								
MRAM nonvolatile data retention (years)								
MRAM write endurance (read/write cycles)								
MRAM endurance – tunnel junction reliability (years at bias) [17]								
B2. Spin-Torque Transfer (STT) MRAM								
Year of Production	2021	2022	2023	2024	2025	2026	2027	2028
MRAM technology node F (nm) [18]	32	32	22	22	22	16	16	16
MRAM cell size area factor a in multiples of F2	10	10	8	8	8	8	8	8
MRAM typical cell size (um2)	0.010	0.010	0.004	0.004	0.004	0.002	0.002	0.002
MRAM materials technology (In -plane Magnetic Anisotropy (IMA) or Perpendicular Magnetic Anisotropy (PMA))	PMA	PMA	PMA	PMA	PMA	PMA	PMA	PMA
MRAM switching current (uA) [19]	50	50	35	35	35	30	30	25
MRAM write energy (pJ/bit) [20]	0.3	0.3	0.18	0.18	0.18	0.15	0.15	0.15
MRAM active area per cell (um2) [21]	0.003	0.0020	0.0016	0.0012	0.0011	0.0008	0.0008	0.0006
MRAM resistance-area product (Ohm-um2) [22]	10	10	10	9	8	7	7	6
MRAM magnetoresistance ratio (%) [23]	150	150	150	180	180	200	200	200
MRAM nonvolatile data retention (years) [24]	>10	>10	>10	>10	>10	>10	>10	>10
MRAM write endurance (read/write cycles) [25]	>1E15	>1E15	>1E15	>1E15	>1E15	>1E15	>1E15	>1E15
MRAM endurance-tunnel junction reliability (years at bias)	>10	>10	>10	>10	>10	>10	>10	>10

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