UNIVERSITY OF CAMBRIDGE

Solid State Devices

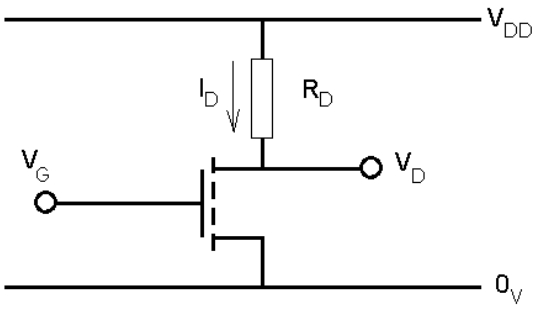
4B6

Lecture 5 – MOSFET (ii)

Daping Chu

Lent 2016

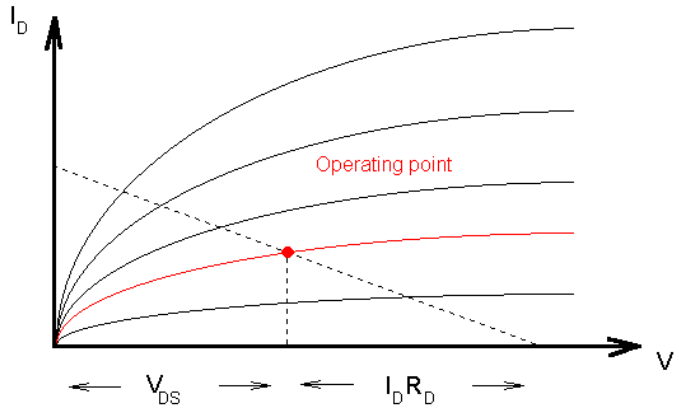
Small signal equivalent circuit – low frequency



Consider an n-channel enhancement mode MOSFET in a common source amplifier with resistive load.

Small signal equivalent circuit – low frequency

Superposing the load line due to $\mathbf{R_D}$ and $\mathbf{V_{DD}}$ on the MOSFET characteristics



Small signal equivalent circuit – low frequency

In the vicinity of the operating point we linearise the output characteristics:

$$I_D(V_{DS}+\delta V_{DS}, V_{GS}+\delta V_{GS}) \approx$$

$$I_D(V_{DS}, V_{GS}) + \delta V_{DS}\left(\frac{\delta I_D}{\delta V_{DS}}\right) + \delta V_{GS}\left(\frac{\delta I_D}{\delta V_{GS}}\right)$$

For small signals (note the use of lower case subscripts) this gives

$$i_d \approx v_{ds}\left(\frac{\delta I_D}{\delta V_{DS}}\right) + v_{gs}\left(\frac{\delta I_D}{\delta V_{GS}}\right)$$

Small signal equivalent circuit – low frequency

$$i_d \approx v_{ds}\left(\frac{\delta I_D}{\delta V_{DS}}\right) + v_{gs}\left(\frac{\delta I_D}{\delta V_{GS}}\right)$$

The partial derivatives are both dimensionally conductance.

$$\left(\frac{\delta I_D}{\delta V_{DS}}\right) = \frac{1}{r_d} \qquad \left(\frac{\delta I_D}{\delta V_{GS}}\right) = g_m$$

$\mathbf{r_d}$ = drain resistance;

$\mathbf{g_m}$ = mutual conductance; – It relates the current in one place to a voltage in another (output ***I*** related to input ***V***).

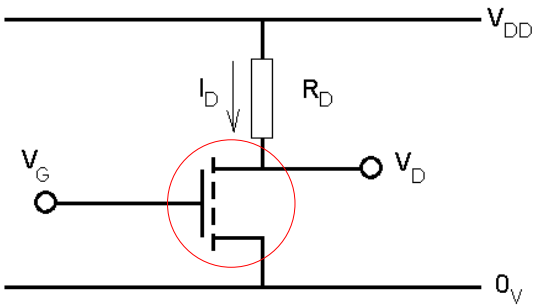
So that

$$i_d \approx v_{ds}\frac{1}{r_d} + v_{gs}g_m$$

Small signal equivalent circuit – low frequency

$$i_d \approx v_{ds}\frac{1}{r_d} + v_{gs}g_m$$

The two currents are <u>added</u> for $\mathbf{i_d}$, so that there are <u>parallel</u> current paths in the equivalent circuit for the FET.

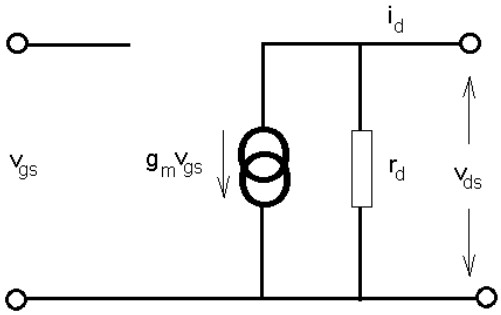


Actual circuit

Small signal equivalent circuit – low frequency

$$i_d \approx v_{ds}\frac{1}{r_d} + v_{gs}g_m$$

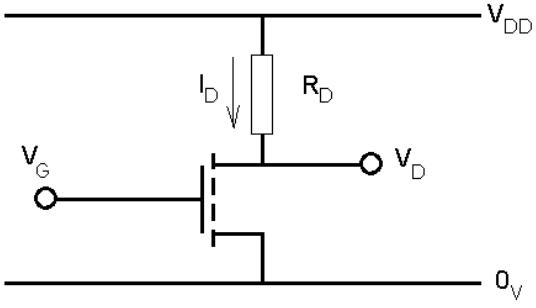
The two currents are <u>added</u> for $\mathbf{i_d}$, so that there are <u>parallel</u> current paths in the equivalent circuit for the FET.



Equivalent circuit

Small signal equivalent circuit – low frequency

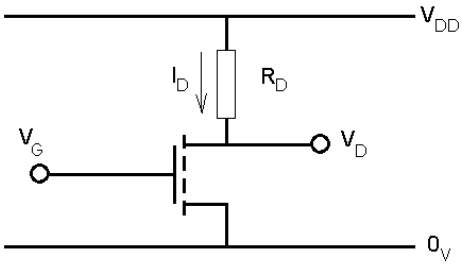
Quiescent values	total	signal
$\mathbf{V_{DS}}$	$\mathbf{V_{DS} + v_{ds}}$	$\mathbf{v_{ds}}$
$\mathbf{V_{GS}}$	$\mathbf{V_{GS} + v_{gs}}$	$\mathbf{v_{gs}}$
$\mathbf{I_D}$	$\mathbf{I_D + i_d}$	$\mathbf{i_d}$
$\mathbf{V_{DD}}$	$\mathbf{V_{DD} + 0}$	$\mathbf{0}$



Total signal is operating point (quiescent value) plus signal.

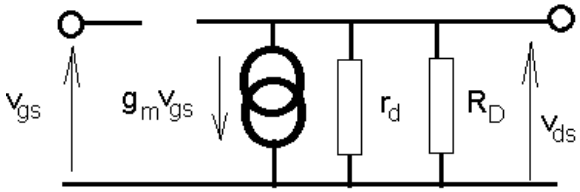
Supply rail is equivalent to ground for small signals.

Small signal equivalent circuit – low frequency



Current in generator equal and opposite to total current in drain and load resistors

Equivalent circuit including load resistor



Small signal equivalent circuit – low frequency

$$i_d \approx v_{ds}\frac{1}{r_d} + v_{gs}g_m$$ small signal drain current.

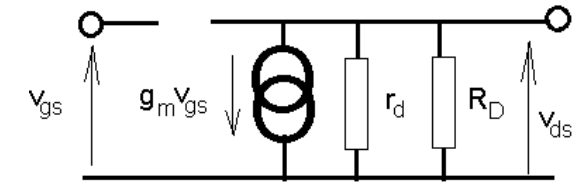
Current in generator equal and opposite to total current in drain and load resistors

$$g_m v_{gs} = -v_{ds}\left(\frac{1}{r_d} + \frac{1}{R_D}\right)$$

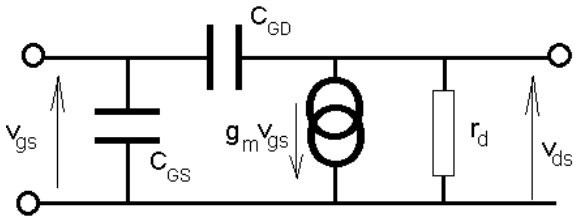
$$\frac{v_{ds}}{v_{gs}} = -g_m \frac{r_d R_D}{(r_d + R_D)}$$ for the voltage gain.

Small signal equivalent circuit – high frequency

At high frequencies add stray capacitances to low frequency model:



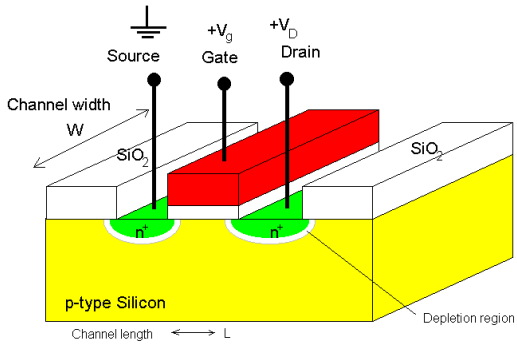
Low frequency equivalent circuit



High frequency equivalent circuit

Small signal equivalent circuit – high frequency

Assume gate length matches channel length ie. no gate overlap with source or drain, also long gate, neglect fringing fields.



Then

$$C_{GS} = LWC_{ox}$$

(substrate at source potential)

Small signal equivalent circuit – high frequency

Assume $C_{GD} = 0$ then $i_g = v_{gs} j\omega LW C_{ox}$

and $i_d = v_{gs} g_m$

If the current gain falls to unity at frequency f_T then

$$g_m v_{gs} = \left| v_{gs} j\omega LW C_{ox} \right|$$

So that $g_m = 2\pi f_T LW C_{ox}$

Small signal equivalent circuit – high frequency

But $g_m = \frac{\mu W C_{ox} V_D}{L}$ in the linear region,

so $2\pi f_T LW C_{ox} = \frac{\mu W C_{ox} V_D}{L}$

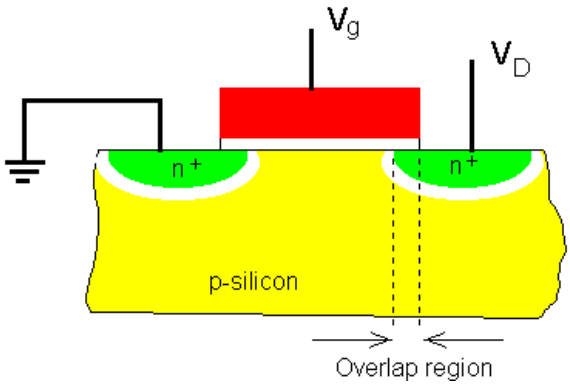
Hence $f_T = \frac{\mu V_D}{\left(2\pi L^2\right)} = \frac{1}{2\pi} \frac{\mu V_D}{L} \frac{1}{L}$

So that a high mobility and a short gate length are important for high frequency operation.

Miller effect

C_{GD} depends on the gate-drain overlap.

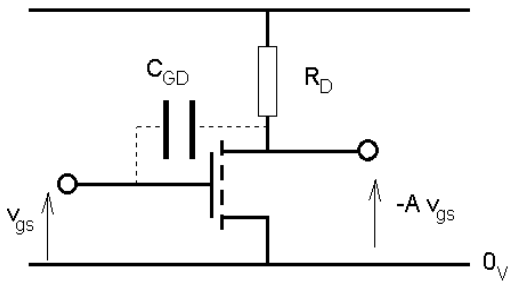
The magnitude of the overlap depends on the details of the fabrication process.



Miller effect

Inverting amplifier with gain **A** and Miller capacitance **C_{GD}** and signal across **C_{GD}** is **v_{gs}(1 + A)**.

Input current due to **C_{GD}** : $i_g = v_{gs}(1+A)j\omega C_{GD}$



Miller effect

The current into the gate is such that its as if the device had an additional capacitance to ground of

$$(1 + A)\, C_{GD}.$$

This degrades the input impedance at high frequency.

Input capacitance is now

$$C_{GS} + (1 + A)\, C_{GD}.$$

Since the effective drain capacitance is multiplied by the gain (may be very large), it is important to minimise C_{GD} by limiting the gate-drain overlap.

MOSFET non-ideal factors

1. Non-zero flat band voltage

$$V_{FB} = \phi_{ms} - \frac{Q_0}{C_{ox}}$$

which incorporates the deviations from ideal MOS capacitor behaviour due to materials (gate polysilicon doping) and processing effects (oxide charge).

These effects are accounted for in a simple manner through the modified threshold voltage

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{(2\psi_B)2\varepsilon_0\varepsilon_s eN_A}}{C_{ox}}$$

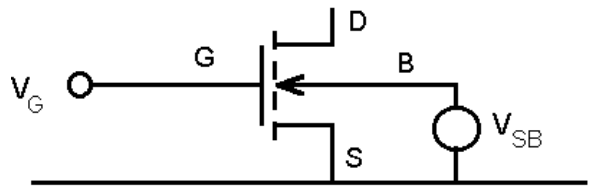
MOSFET non-ideal factors

2. Substrate bias

Substrate connection B no longer at the source potential.

For n-channel devices, with the substrate negative w.r.t. source, the depletion layer width increases, so increasing the depletion charge.

Gate voltage must be increased to compensate for this effect, leading to a higher threshold voltage $\mathbf{V_T}$.

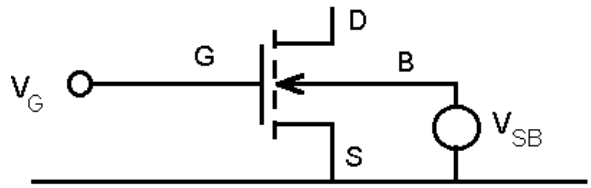


MOSFET non-ideal factors

2. Substrate bias

The modified threshold voltage $\mathbf{V_T}$ Is given by

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{\left(2\psi_B + |V_{sub}|\right) 2\varepsilon_0 \varepsilon_s e N_A}}{C_{ox}}$$



MOSFET non-ideal factors

3. Diffusion current

Definition of threshold voltage V_T based on arbitrary choice for onset of strong inversion.

Channel is weakly inverted at $V_G<V_T$, for $\Psi_B<\Psi_S<2\Psi_B$.

In weak inversion, $V_G<V_T$ (sub-threshold condition).

Now drain current dominated by diffusion, this is similar to the collector current in a bipolar transistor.

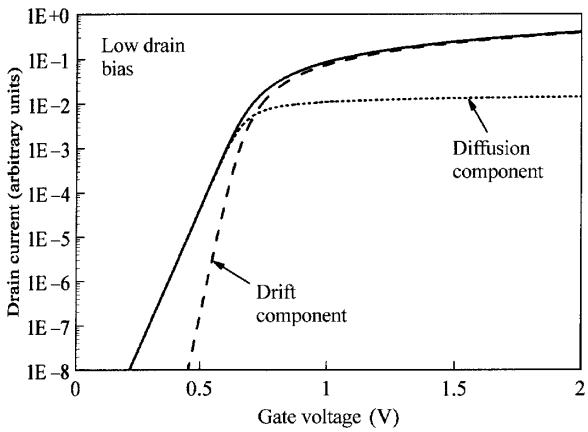
Sub-threshold current varies exponentially with gate voltage.

This effect increases the sub-threshold current.

MOSFET non-ideal factors

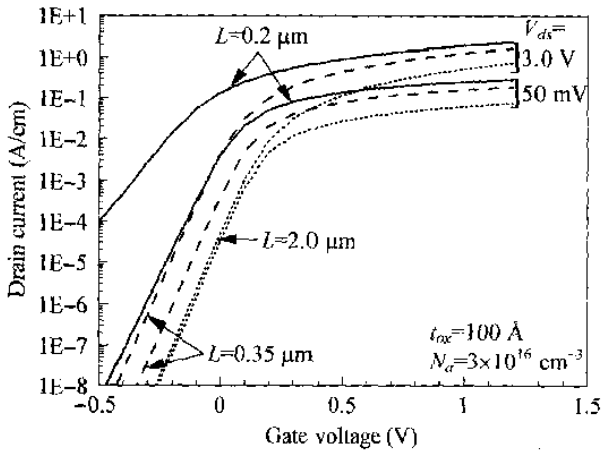
3. Diffusion current

Previously, only drift current considered (channel in strong inversion).



MOSFET non-ideal factors

3. Diffusion current

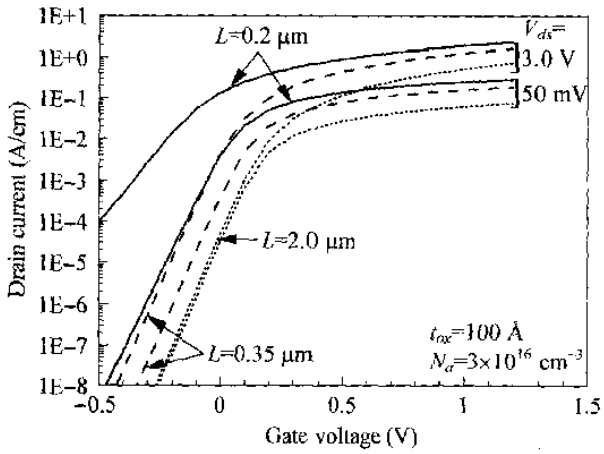


As the channel length decreases, the depletion region of the drain starts to interact with the source-channel junction to lower the source junction potential barrier.

This allows electrons to be injected into the channel regardless of the gate voltage.

MOSFET non-ideal factors

3. Diffusion current

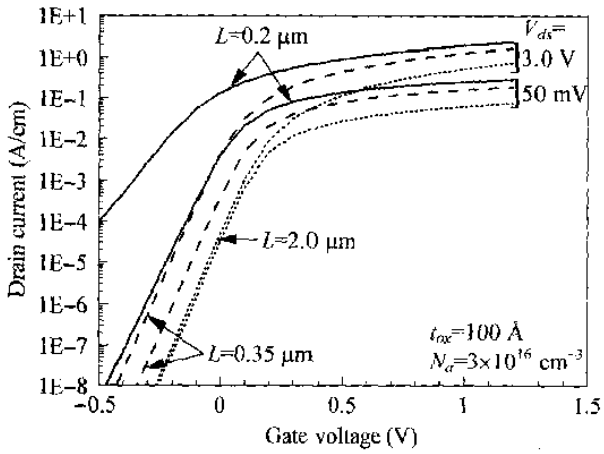


Drain acts as a sink for electrons, the current in the channel flows by diffusion in the sub-threshold region, similar to the flow in a bipolar transistor.

Above threshold the current flow is predominantly by drift.

MOSFET non-ideal factors

3. Diffusion current



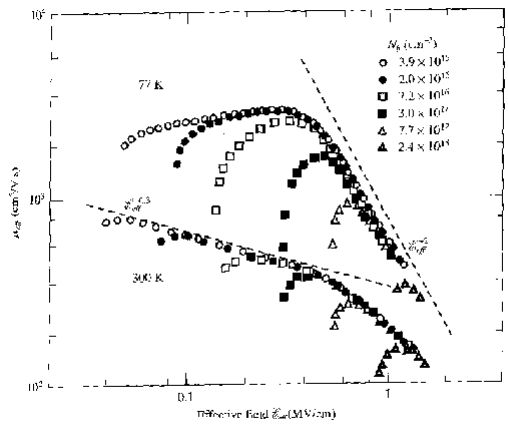
Channel needs heavier doping to counteract this effect.

Important for large $\mathbf{V_{DD}}$ and short channel lengths.

MOSFET non-ideal factors

4. Non-uniform mobility

Electron velocity not proportional to electric field at high longitudinal electric fields.



$\mathbf{I_D}$ reduced due to velocity saturation, effect is more pronounced at high gate voltages due to increased scattering.

μ is also strongly affected by the doping density, temperature and effective field (the part of the field mainly due to the gate voltage).

MOSFET non-ideal factors

5. Ion implant to control $\mathbf{V_T}$

Implantation at low energy (ie close to gate oxide) into MOSFET channel.

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{\left(2\psi_B + |V_{sub}|\right) 2\varepsilon_0 \varepsilon_s e N_A}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

where $\mathbf{Q_I}$ is the implanted charge.

Note here: $V_{FB} = \Phi_{ms} - \frac{Q_o}{C_{ox}}$

MOSFET non-ideal factors

6. Short channel effects

Benefits from reducing MOSFET size:

- improved circuit performance as maximum frequency is increased through reduction in capacitance (depends on area).
- increased circuit size/complexity.

However, MOSFET behaviour is modified by short channel effects.

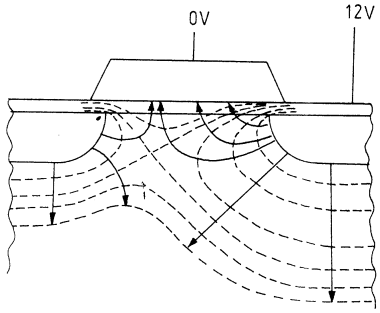
Particularly, reliability and sub-threshold current.

MOSFET non-ideal factors

6. Short channel effects

(i) Channel length modulation and punch-through breakdown.

The gradual channel model is 1-dimensional, but real electric fields are 2-dimensional and so we cannot assume that the vertical fields >>in-plane fields.



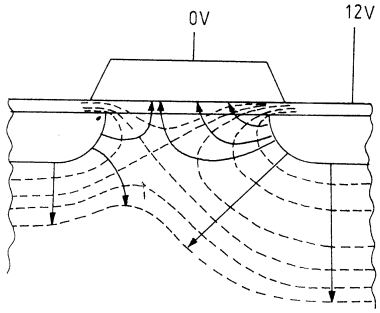
MOSFET non-ideal factors

6. Short channel effects

(i) Channel length modulation and punch-through breakdown.

The depletion layer around the drain contact penetrates under the gate as $\mathbf{V_D}$ increases so shortening the effective channel length.

So that for a given $\mathbf{v_{gs}}$, $\mathbf{I_D}$ is greater than in the gradual channel model.



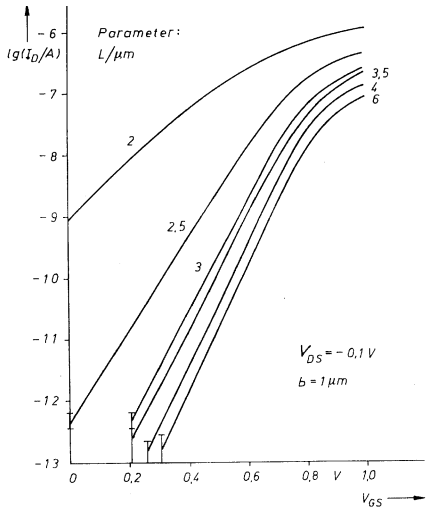
MOSFET non-ideal factors

6. Short channel effects

(i) Channel length modulation.

Effect becomes more important as the gate length is reduced as the depletion layer thickness becomes a larger proportion of the channel length.

Particularly important for sub-threshold slope.

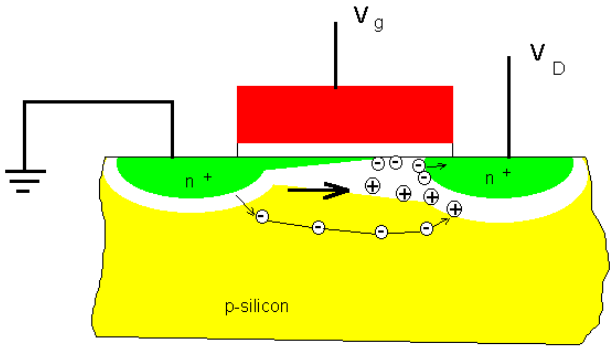


MOSFET non-ideal factors

6. Short channel effects

(i) Punch-through breakdown.

As the effective channel length shortens, current depends exponentially on the source-drain voltage due to lowering of potential barrier in the channel region.

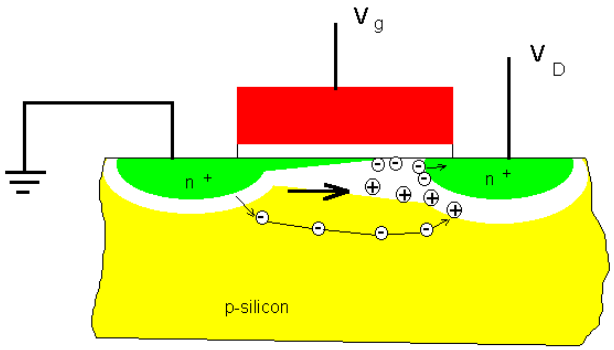


MOSFET non-ideal factors

6. Short channel effects

(i) Punch-through breakdown.

Electrons are accelerated across the depleted channel and the gate loses control of the drain current. This eventually leads to breakdown between the source and drain known as punch-through.

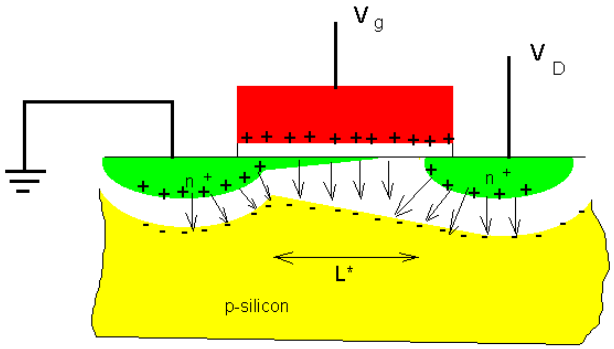


MOSFET non-ideal factors

6. Short channel effects

(ii) Change of threshold voltage.

Another consequence of the 2-D field distribution.



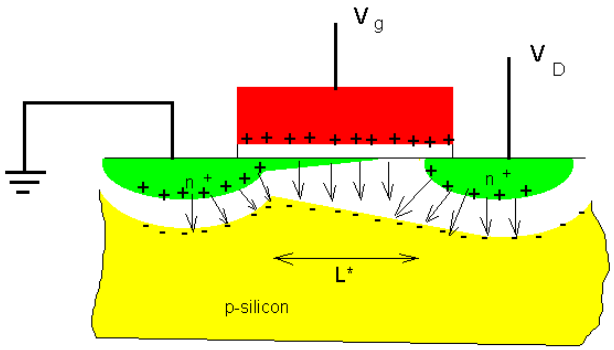
Gate, source and drain voltages all influence the depletion layer.

MOSFET non-ideal factors

6. Short channel effects

(ii) Change of threshold voltage.

Part of the depletion layer charge lying under the gate is influenced by the source $\mathbf{Q_{source}}$ and drain $\mathbf{Q_{drain}}$ charge.



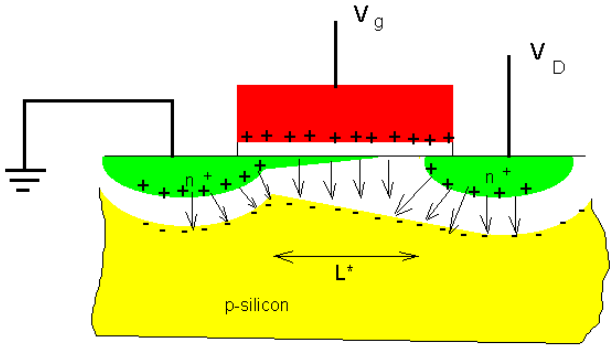
So that $\mathbf{Q_{gate}}$ < charge in depleted channel and $\mathbf{V_G}$ is less than the predicted long channel model value for a given $\mathbf{I_D}$.

MOSFET non-ideal factors

6. Short channel effects

(ii) Change of threshold voltage.

As the gate length is made shorter these short channel effects shift the threshold voltage and increase the sub-threshold current reducing the ability to turn off the device.



MOSFET non-ideal factors

6. Short channel effects

(iii) Hot carrier effects.

Large voltages and short gate lengths lead to a high electric field in the depletion region at the channel drain junction. Carriers in this region may acquire velocities substantially larger than the thermal velocity ie. hot carriers, leading to:

carrier injection into the gate oxide

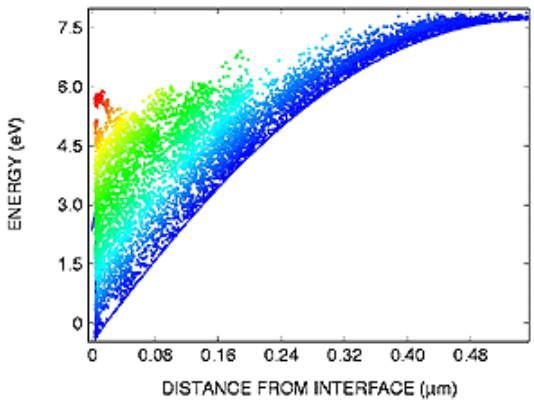
electron-hole pair generation (impact ionisation)

MOSFET non-ideal factors

6. Short channel effects

(iii) Hot carrier effects.

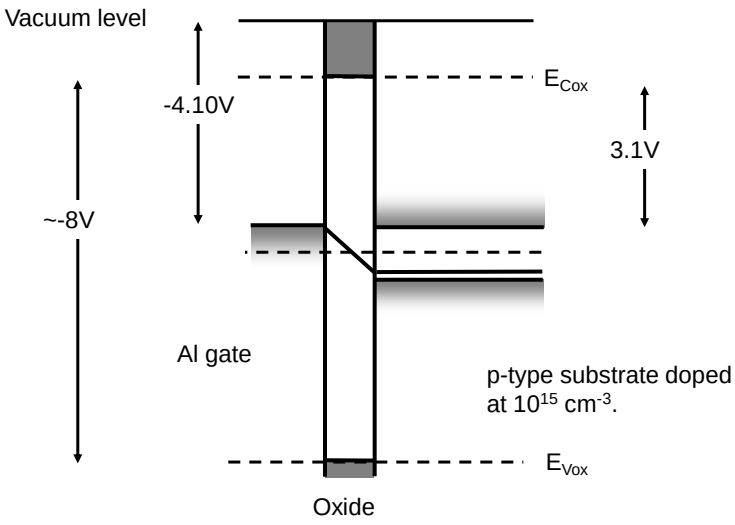
These carriers are strongly attracted by the gate potential; such injection leads to an increased gate leakage current and oxide charge.



Carrier injection into the gate oxide is possible for carriers with energy > ~ 1.5eV.

Blue is cold, red is hot.

Non-ideal MOS capacitor

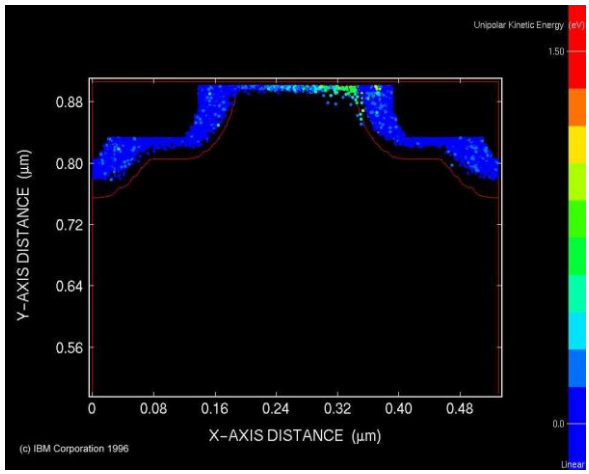


The potential barrier between the conduction bands in silicon and silicon dioxide is only 3.1eV.

MOSFET non-ideal factors

6. Short channel effects

(iii) Hot carrier effects.



n-channel MOSFET

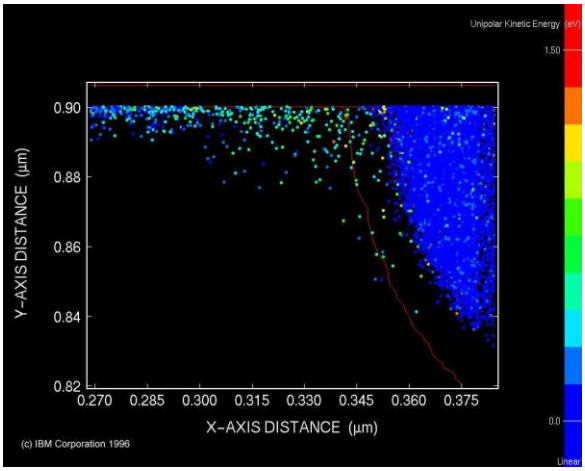
Carrier energy in channel and around source and drain contacts.

Blue is cold, red is hot.

MOSFET non-ideal factors

6. Short channel effects

(iii) Hot carrier effects.

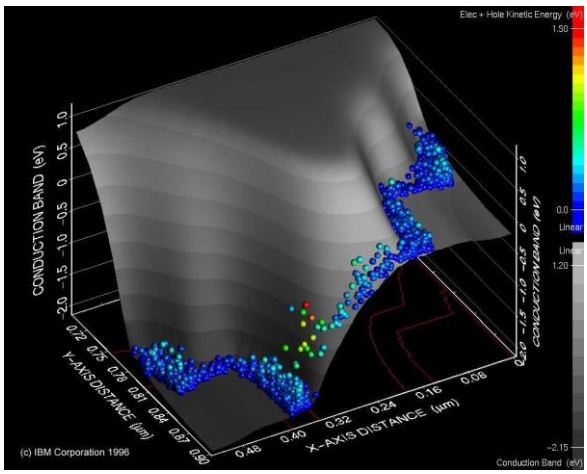


Close to the drain end some lucky electrons gain far more energy than the local potential suggests.

MOSFET non-ideal factors

6. Short channel effects

(iii) Hot carrier effects.



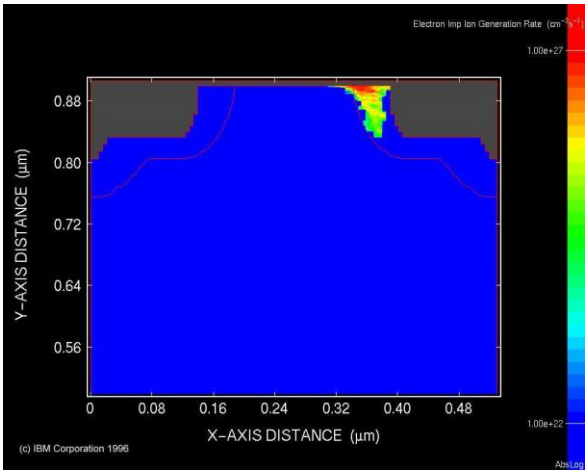
Pseudo 3-D view looking into substrate from oxide silicon interface.

Some electrons are very hot at the drain end.

MOSFET non-ideal factors

6. Short channel effects

(iii) Hot carrier effects.



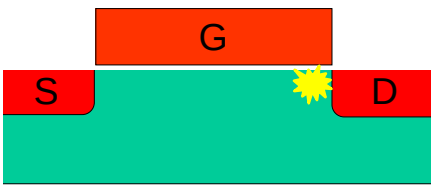
This causes significant impact ionisation at the drain end.

MOSFET non-ideal factors

6. Short channel effects

(iii) Hot carrier effects.

Electron-hole pair generation occurs by impact ionisation and can lead to avalanche breakdown.



MOSFET non-ideal factors

6. Short channel effects

(iii) Hot carrier effects.

Electron-hole pair generation occurs by impact ionisation and can lead to avalanche breakdown.

These deleterious effects can be counteracted by reducing the drain doping density (lightly doped drain LDD) to reduce the electric field close to the drain.