UNIVERSITY OF CAMBRIDGE

Solid State Devices

4B6

Lecture 4 – MOSFET (i)

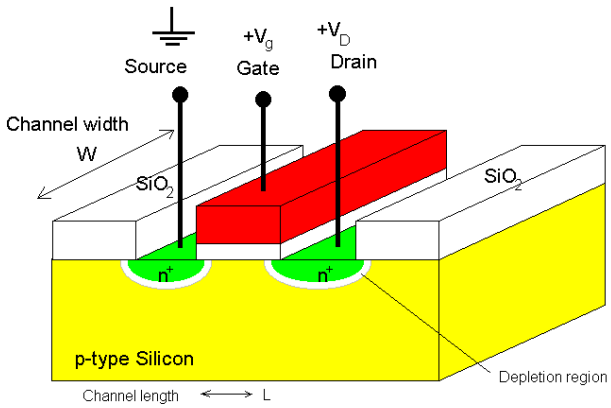
Daping Chu

Lent 2016

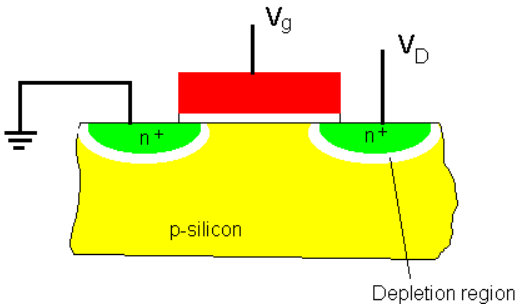
MOSFET simple analysis

We consider a simplified MOSFET structure with the source grounded and the bulk floating.

The voltages applied to the gate and the drain determine the carrier density and the level of conduction in the channel (ideal MOS capacitor).

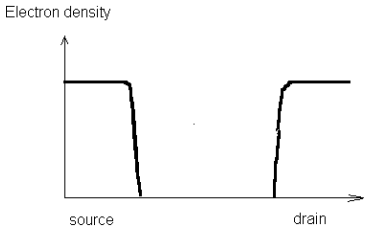


MOSFET simple analysis



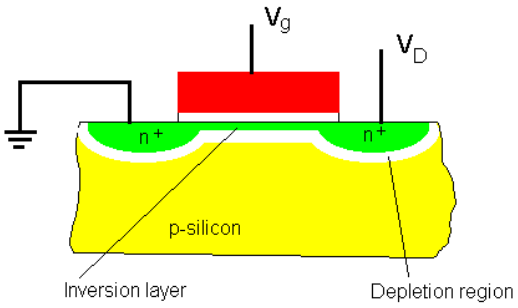
V_g=0, V_D=0

Source and drain highly n-doped contacts isolated from lightly p-doped substrate by depletion regions.



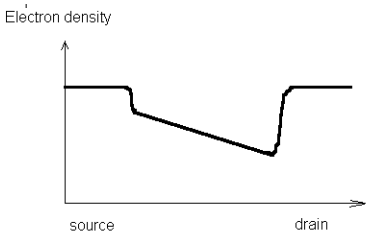
No inversion layer (V_g>0), hence no conduction between source and drain.

MOSFET simple analysis



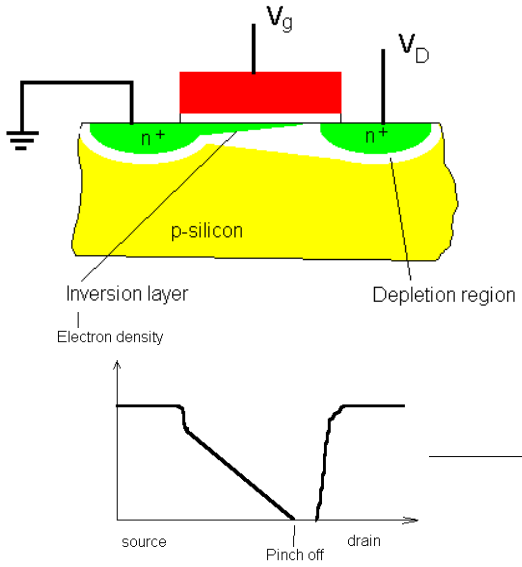
V_g=V_T, V_D>0 (but small)

Inversion layer created in channel, hence conduction between source and drain.



Carrier concentration in channel is higher at source end than at drain end (V_g-V_D across MOS capacitor).

MOSFET simple analysis



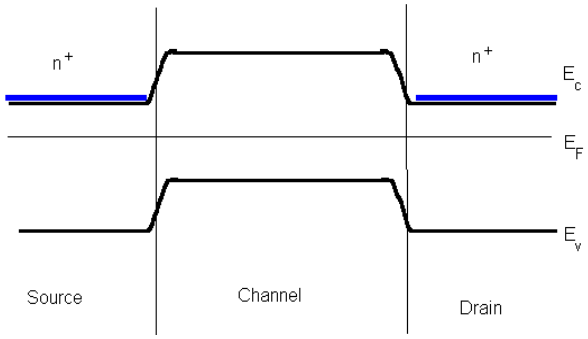
$V_g > V_T$, $V_D > V_{Dsat}$ leading to $I_D = I_{Dsat}$

Increasing potential difference between channel and substrate increases depletion width at drain end.

Eventually the channel is pinched-off, but conduction still possible (transient electron population).

Band structure in silicon adjacent to oxide layer

Simple behaviour may be understood by considering the band structure in the silicon where the channel is formed.



V_g=**0**, (flat band) V_D=0, equilibrium ie I_D = 0.

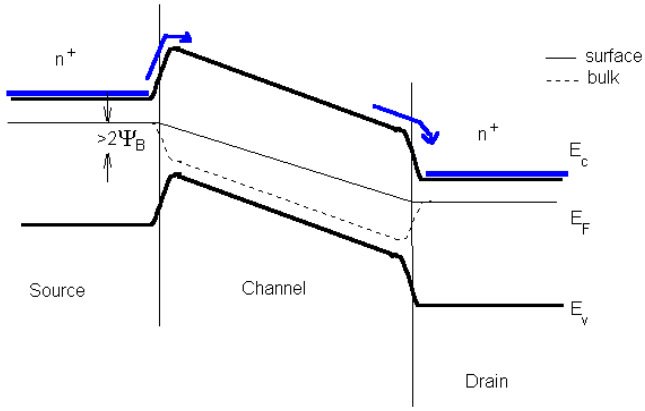
E_F close to conduction band edge in contacts.

E_F energy closer to valence band edge in channel.

No free electrons in channel.

Band structure in silicon adjacent to oxide layer

V_g>0, **V_D**>0 (but small), leading to resistive drop in channel.



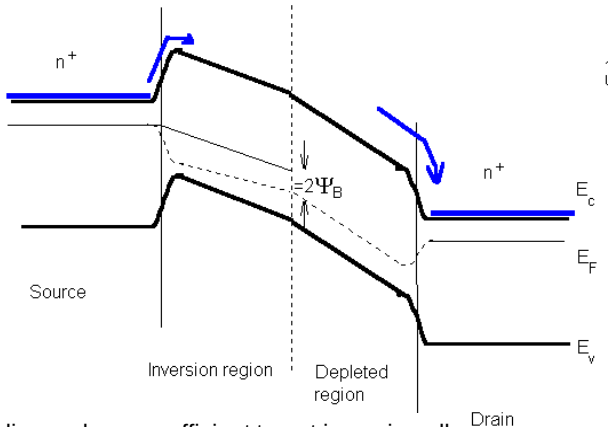
E_F closer to conduction band edge in channel near to surface.

E_F energy closer to valence band edge lower down.

Some electrons overcome barrier and transfer to drain.

Band structure in silicon adjacent to oxide layer

V_{gs}>V_T, **V_{gD}>V_T** leading to **I_D = I_{Dsat}**

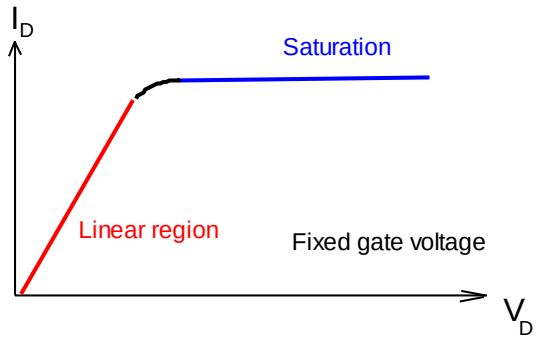


Band bending no longer sufficient to get inversion all along channel near to surface.

Electron population stable only up to edge (but can't get back) so carry on to drain.

MOSFET simple analysis.

I_D-V_D characteristic

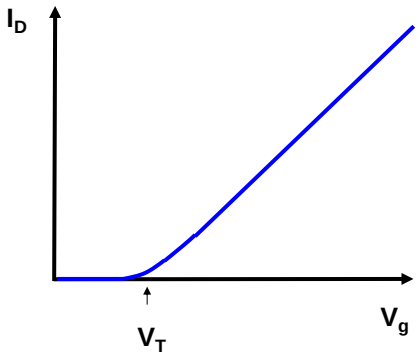


Linear region occurs at low drain voltages where the channel is continuous between the source and the drain.

At larger drain voltages the channel is no longer inverted at the drain end so that the current no longer increases in response to a larger drain voltage.

MOSFET simple analysis.

I_D-V_g characteristic

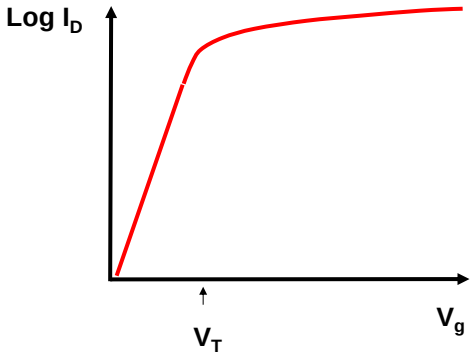


On a linear scale I_D simply increases with increasing V_g above V_T, as expected from the previous analysis.

Below V_T, the current is expected to be zero.

MOSFET simple analysis.

I_D-V_g characteristic



On a log scale I_D is seen to deviate from this behaviour at low gate voltages, particularly below V_T, where simple analysis predicts I_D=zero.

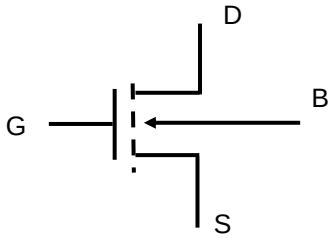
Types of MOSFET

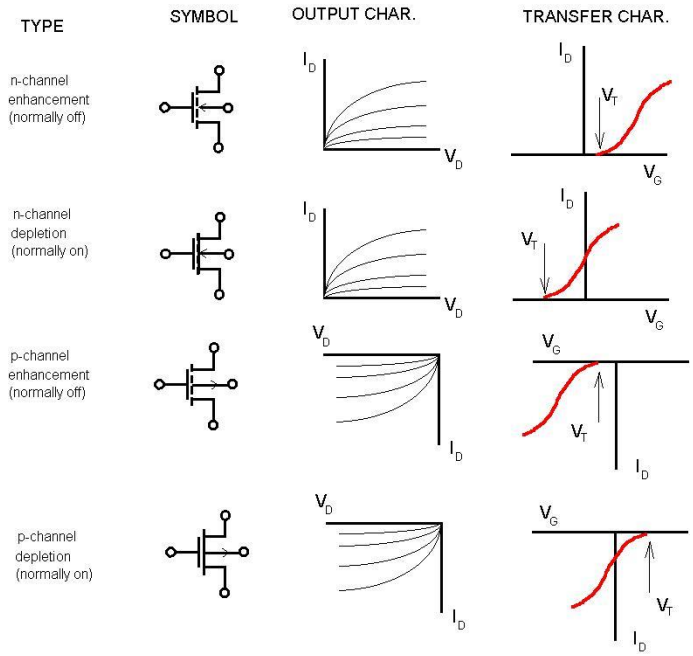
Simple description for n-channel MOSFET with no channel present at zero gate voltage

Four possible choices depending on channel type (n-channel or p -channel) and threshold voltage with respect to drain voltage range (enhancement or depletion).

This wide range of choice give circuit designers great flexibility.

Conventional symbols.....





Simple analysis

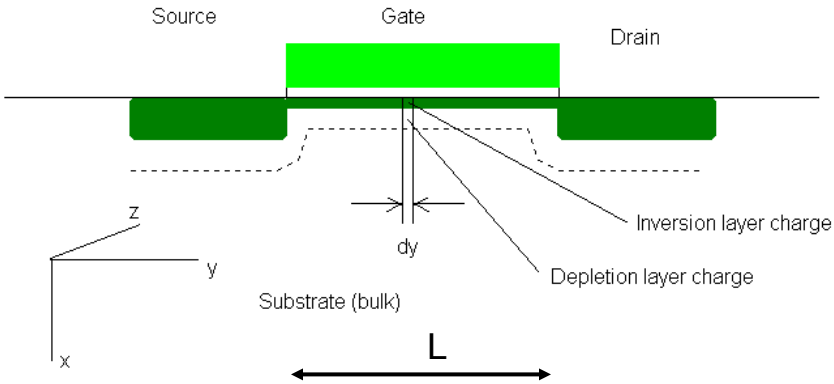
Inversion layer continuous from source to drain. $\mathbf{I_D}$ depends on:

$\mathbf{Q_n}$	areal charge density in inversion layer.
$\boldsymbol{\mu}$	carrier mobility in inversion layer.
dV/dy	potential gradient along channel.

Assumptions:

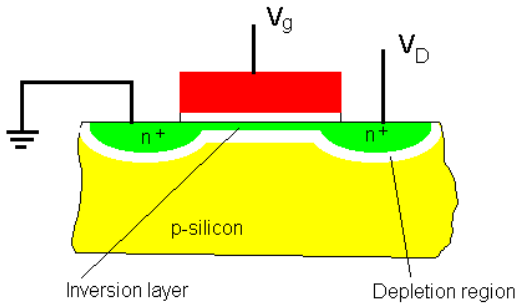
(1) Ideal MOS capacitor.
(2) Constant carrier mobility in inversion layer.
(3) Uniform doping in substrate.
(4) No reverse leakage current (to undepleted substrate).
(5) Drift current only.
(6) Axial electric field >> longitudinal electric field.

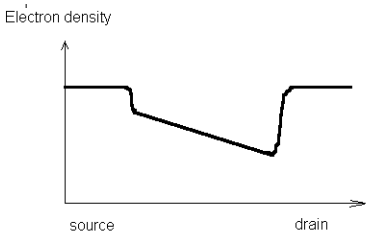
Gradual channel approximation



Inversion layer charge $\mathbf{Q_n}$.
Depletion layer charge $\mathbf{Q_B}$.
Channel length **L**.
Channel width **z**.

MOSFET simple analysis





Charge at channel surface –

is due to combination of inversion charge Q_n and depletion charge Q_B.

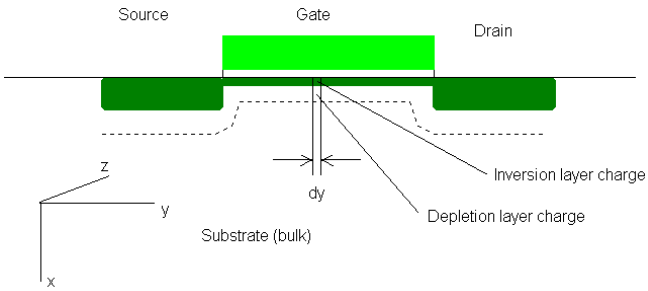
depends on position since voltage across capacitor varies from source to drain.

Gradual channel approximation

Surface charge density at y:

$$Q_s(y) = C_{ox} V_{ox}(y) = [\psi_s(y) - V_G] C_{ox}$$

where $\mathbf{C_{ox}}$ is the oxide cap. and $\mathbf{V_{ox}}$ is the voltage across the oxide.

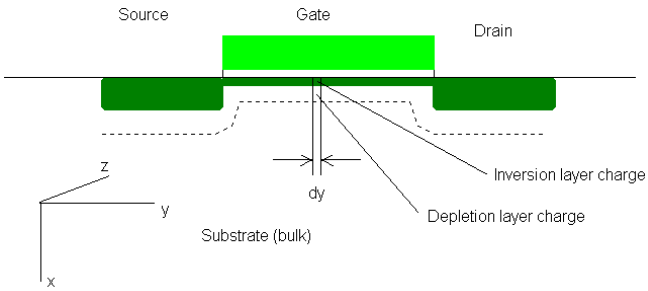


Gradual channel approximation

Inversion layer charge:

$$Q_n(y) = Q_s(y) - Q_B(y) = -[V_G - \psi_s(y)] C_{ox} - Q_B(y)$$

where $\mathbf{Q_B(y)}$ is the bulk charge (ionised acceptors) in the depletion layer.



Gradual channel approximation

At inversion,

$$\psi_s(y) \approx 2\psi_B + V(y)$$

From the MOS capacitor, the depletion width **w** is given by

$$w = \sqrt{\frac{2\varepsilon_s \psi(inv)}{eN_A}}$$

So we get

$$Q_B(y) = -eN_A w = -\sqrt{2e\varepsilon_s N_A [2\psi_B + V(y)]}$$

Gradual channel approximation

Therefore the inversion layer charge is

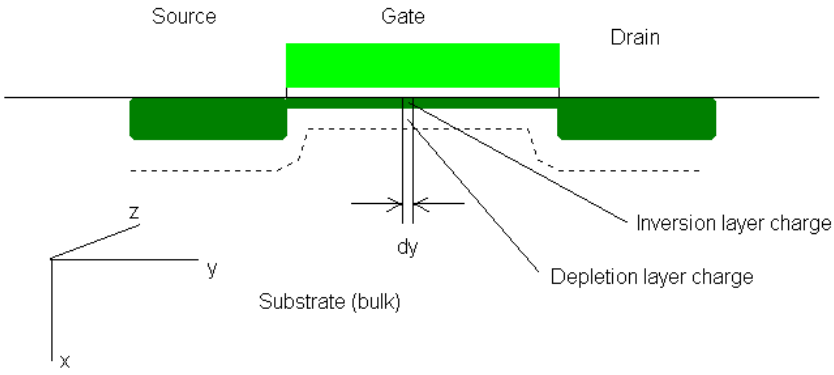
$$Q_n(y) = -[V_G - V(y) - 2\psi_B]C_{ox} + \sqrt{2e\varepsilon_s N_A [2\psi_B + V(y)]}$$

This inversion layer charge gives rise to a current given by:

mobility X charge per unit area X electric field X channel width

$$I = \mu_n |Q_n| \frac{dV}{dy} z$$

Gradual channel approximation



Current flow is continuous from source to drain but voltage drop depends on surface potential.

Need to integrate separate contributions to get total voltage drop for given current.

Gradual channel approximation

$$I = \mu_n |Q_n| \frac{dV}{dy} z$$ but **dV=I.dR**

So that the resistance **dR** of a slice **dy** is $dR = \frac{dy}{z\mu_n |Q_n|}$

So that

$$Idy = z\mu_n |Q_n(y)| dV$$

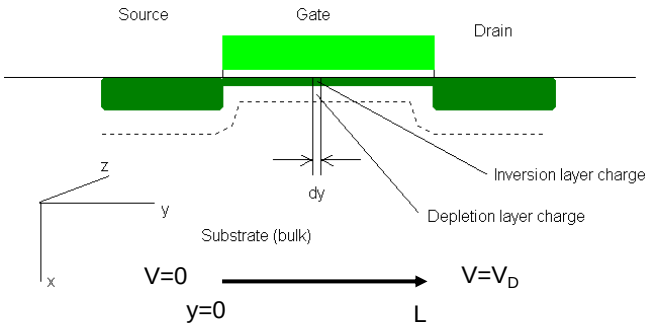
Substituting

$$Idy = z\mu_n \left\{ [V_G - V(y) - 2\psi_B] C_{ox} - \sqrt{2e\varepsilon_s N_A [2\psi_B + V(y)]} \right\} dV$$

Gradual channel approximation

Integrating **y** from 0 to **L** ie. **V(y)** from 0 to V_D gives

$$I_D = \frac{z}{L}\mu_n C_{ox}\left\{\left[V_G - 2\psi_B - \frac{V_D}{2}\right]V_D - \frac{2}{3}\sqrt{\frac{2e\varepsilon_s N_A}{C_{ox}}}\left(V_D + 2\psi_B\right)^{\frac{3}{2}} - \left(2\psi_B\right)^{\frac{3}{2}}\right\}$$



Gradual channel approximation

Integrating **y** from 0 to **L** ie. **V(y)** from 0 to V_D gives

$$I_D = \frac{z}{L}\mu_n C_{ox}\left\{\left[V_G - 2\psi_B - \frac{V_D}{2}\right]V_D - \frac{2}{3}\sqrt{\frac{2e\varepsilon_s N_A}{C_{ox}}}\left(V_D + 2\psi_B\right)^{\frac{3}{2}} - \left(2\psi_B\right)^{\frac{3}{2}}\right\}$$

Expanding the final term as a series, for small V_D, V_D^3 and higher powers can be neglected:

$$I_D \approx \frac{z}{L}\mu_n C_{ox}\left\{\left[V_G - V_T\right]V_D - \left(\frac{1}{2} + \frac{\sqrt{e\varepsilon_s N_A/\psi_B}}{4C_{ox}}\right)V_D{}^2\right\}$$

Gradual channel approximation – linear region

$V_D << V_G - V_T$:

$$I_D \approx \frac{z}{L}\mu_n C_{ox}\left[V_G - V_T\right]V_D$$

Channel conductance:

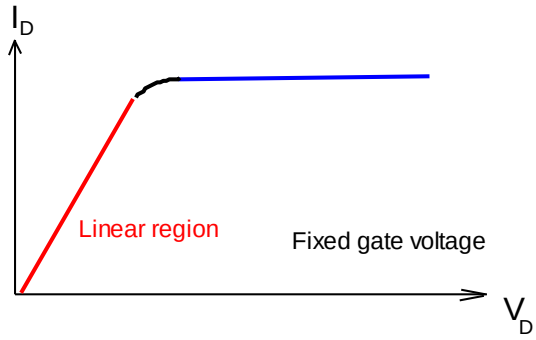
$$g_D = \frac{\delta I_D}{\delta V_D} = \frac{z}{L}\mu_n C_{ox}\left[V_G - V_T\right]$$

Transconductance:

$$g_m = \frac{\delta I_D}{\delta V_G} = \frac{z}{L}\mu_n C_{ox} V_D$$

MOSFET simple analysis

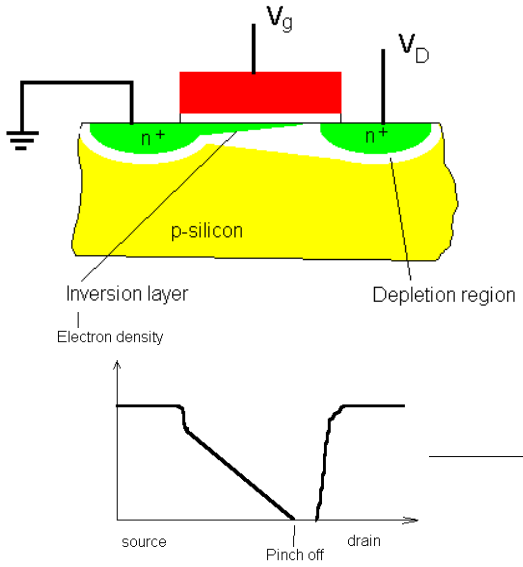
I_D-V_D characteristic



Slope of linear region depends on excess gate drive

$$g_D = \frac{\delta I_D}{\delta V_D} = \frac{z}{L}\mu_n C_{ox}\left[V_G - V_T\right]$$

MOSFET simple analysis



Limit of linear region when pinch-off occurs at drain end for $V_D=V_{Dsat.}$

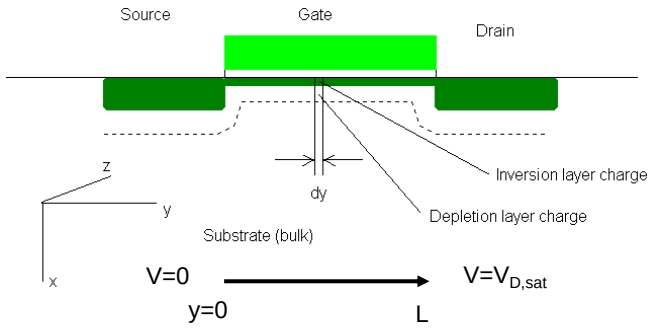
Inversion layer no longer continuous between source and drain.

$V_g>V_T$, $V_D>V_{Dsat}$ leading to $I_D = I_{Dsat.}$

Gradual channel approximation – saturation region

At the onset of saturation, $Q_n(L)=0$.

$$Q_n(L) = -\left[V_G - V_{D,sat} - 2\psi_B\right]C_{ox} + \sqrt{2e\varepsilon_s N_A\left[2\psi_B + V_{D,sat}\right]} = 0$$



Gradual channel approximation – saturation region

So that

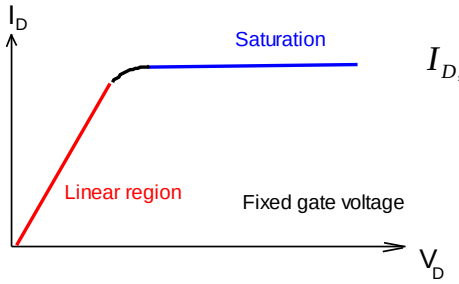
$$\left[V_G - V_{D,sat} - 2\psi_B\right]C_{ox} = \sqrt{2e\varepsilon_s N_A\left[2\psi_B + V_{D,sat}\right]}$$

which can be solved as a quadratic in $\mathbf{V_{D,sat}}$:

$$V_{D,sat} = V_G - 2\psi_B + \left(\frac{e\varepsilon_s N_A}{C_{ox}^{\ 2}}\right)\left(1 - \sqrt{1 + \frac{2V_G C_{ox}^{\ 2}}{e\varepsilon_s N_A}}\right)$$

Gradual channel approximation – saturation region

Substituting into the equation for $\mathbf{I_D}$ and simplifying



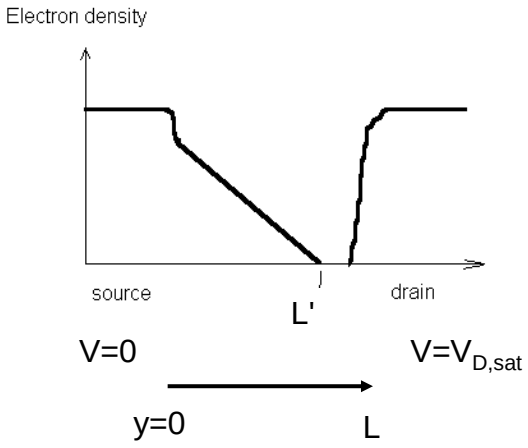
$$I_{D,sat} \approx \frac{z}{2L}\mu_n C_{ox}\left[V_G - V_T\right]^2$$

No dependence on V_D so no conductance (current is fixed) but still a transconductance

$$g_{m,sat} = \frac{\delta I_{D,sat}}{\delta V_G} = \frac{z}{L}\mu_n C_{ox}\left[V_G - V_T\right]$$

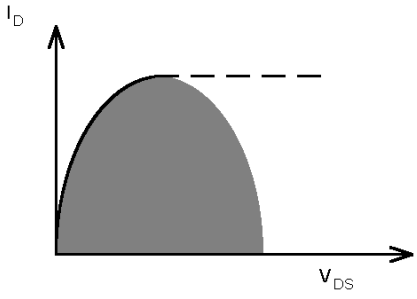
Gradual channel approximation – saturation region

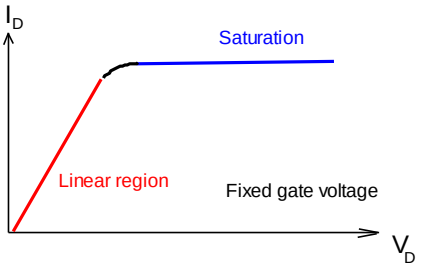
When $\mathbf{V_D}$>$\mathbf{V_{D,sat}}$ the end of the inversion point (L') moves closer to the source.



Gradual channel approximation – saturation region

$\mathbf{Q_n(L')}$=0 for L'<L and $\mathbf{V(L')} = \mathbf{V_{D,sat}}$.

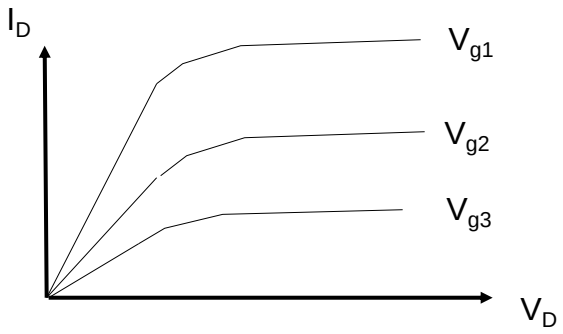




Drain current behaviour is described by a parabola with the vertex displaced from the origin.

Resistance of inversion layer reduces only slightly, so that $\mathbf{dI_D/dV_D=1/r_d}$ is non-zero (increase slope of dashed line).

MOSFET simple analysis



Current essentially independent of V_D in saturation but still depends on gate voltage.

Most important operating region of transistor: $\mathbf{V_g > V_T}$

Worked example

Find the drain current for an n-channel silicon MOSFET, with z/L ratio of 100μm/1μm, operating with drain, gate, source and substrate voltages of 5, 3, 0 and 0V respectively. The gate oxide thickness is 0.1μm, the substrate doping density is $1x10^{15}cm^{-3}$, the channel mobility 500 $cm^2 V^{-1} s^{-1}$ and the threshold voltage is 1V.

To find the drain current we first need to decide whether the transistor is operating in the linear or the saturated regime. The saturated drain voltage is given by

$$V_{D,sat} = V_G - 2\psi_B + \left(\frac{e\varepsilon_s N_A}{C_{ox}^{\ 2}}\right)\left(1 - \sqrt{1 + \frac{2V_G C_{ox}^{\ 2}}{e\varepsilon_s N_A}}\right)$$

The substrate voltage is

$$\Psi_B = \left(\frac{kT}{e}\right)\ln\left(\frac{N_a}{n_i}\right) = 0.3V$$

Worked example

and the oxide capacitance is

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox}}{t_{ox}} = \frac{8.8\times10^{-12}\times3.9}{10^{-7}} = 3.43\times10^{-4}\ Fm^{-2}$$

So that the saturated drain voltage is

$$V_{D,sat} = 3 - 2\times0.3 + 0.14\times(-5.6) \sim 1.6\,V$$

With a drain voltage of 5V the drain current is saturated and so is given by

$$I_{D,sat} \approx \frac{z}{2L}\mu_n C_{ox}\left[V_G - V_T\right]^2 = 3.43\,mA$$