UNIVERSITY OF CAMBRIDGE

Solid State Devices

4B6

Lecture 3 – MOS capacitor (ii)

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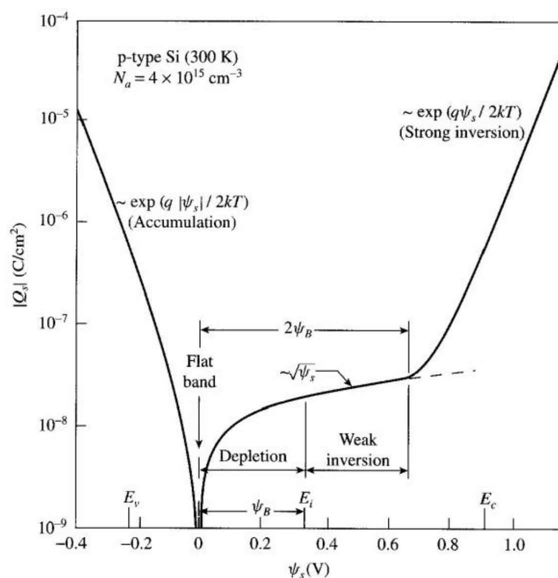
Lent 2016

Control of interface carrier density



Carrier density at oxide silicon interface is strong function of surface potential.

Key to MOSFET technology.

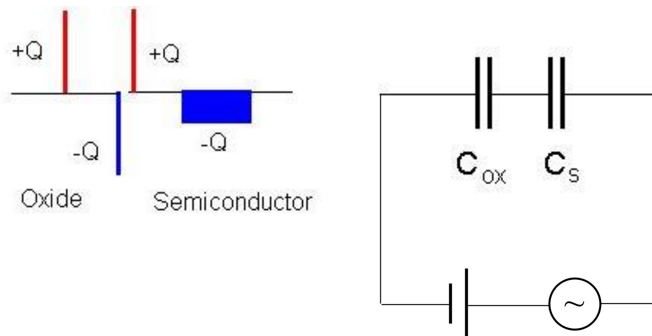
Experimental dependence of MOS capacitance

MOS capacitance found by applying a *small* ac voltage to the device and measuring the out of phase component of the current.

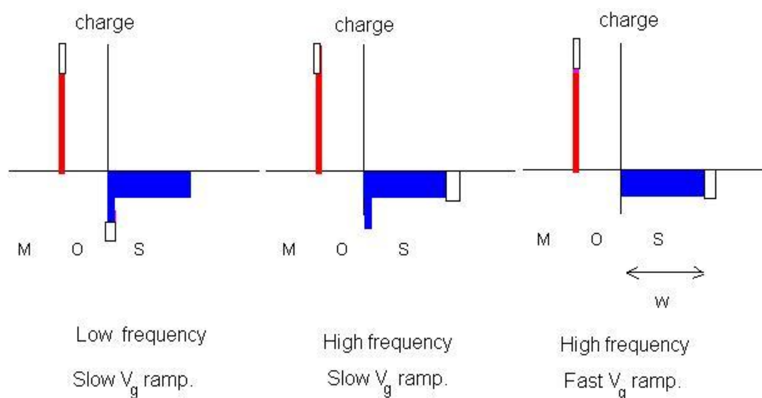
A dc voltage is applied at the same time to control the surface potential, this is known as the ramp voltage, since it is swept in order to observe the change in capacitance with surface potential.

Ideal MOS capacitance in depletion

Any applied voltage appears across the oxide and the depletion layer so that there are, in effect, two capacitors in series, i.e.



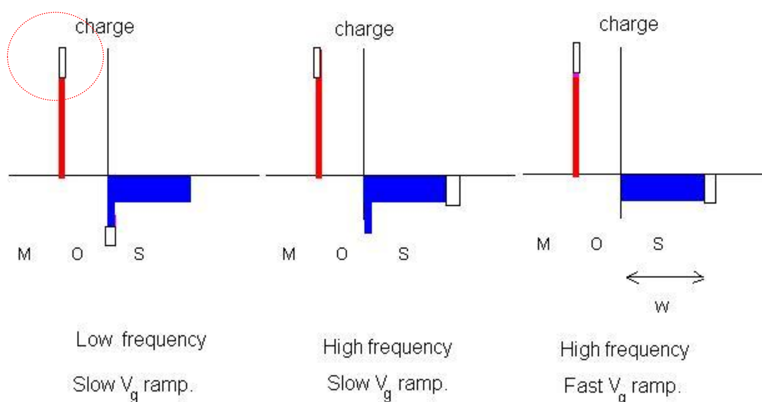
Experimental dependence of MOS capacitance



Three possible measurement regimes:

- low ac frequency + slow ramp
- high ac frequency + slow ramp
- high ac frequency + fast ramp

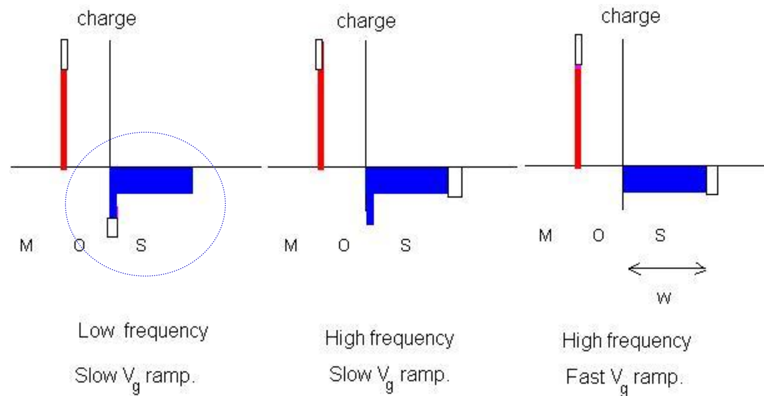
Experimental dependence of MOS capacitance



In all three cases the charge in the metal is able to respond and occupies an infinitely thin layer at the surface.

The response of the charge in the semiconductor is very different.

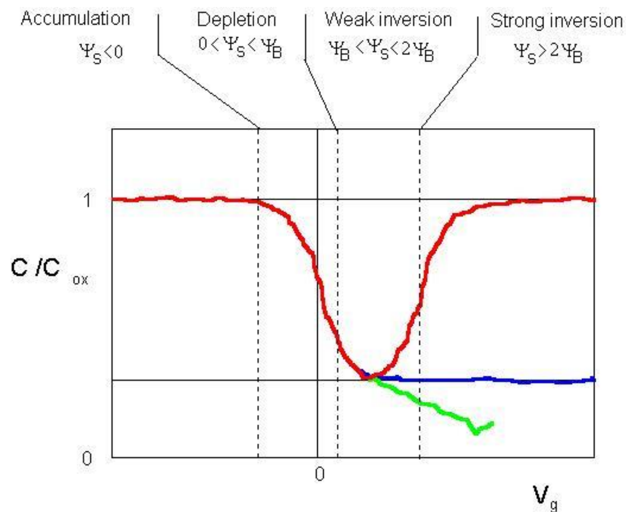
Experimental dependence of MOS capacitance



Low ac frequency + low ramp rate

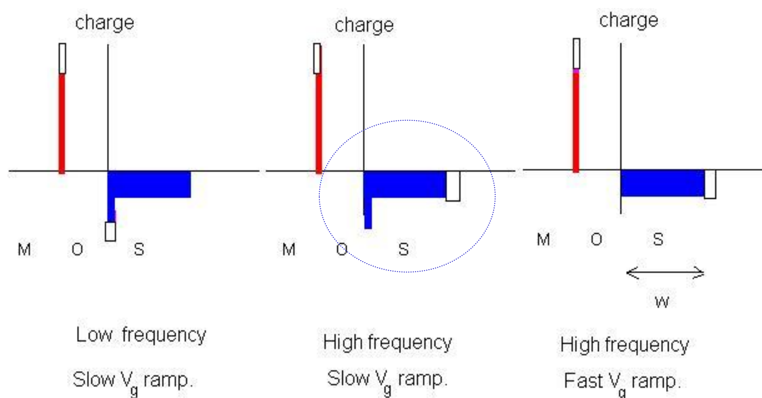
Capacitance due to changes in inversion/accumulation charge in semiconductor in series with oxide capacitance.

Experimental dependence of MOS capacitance



Capacitance due to oxide in accumulation or inversion, but dips between due to additional depletion capacitance in series.

Experimental dependence of MOS capacitance

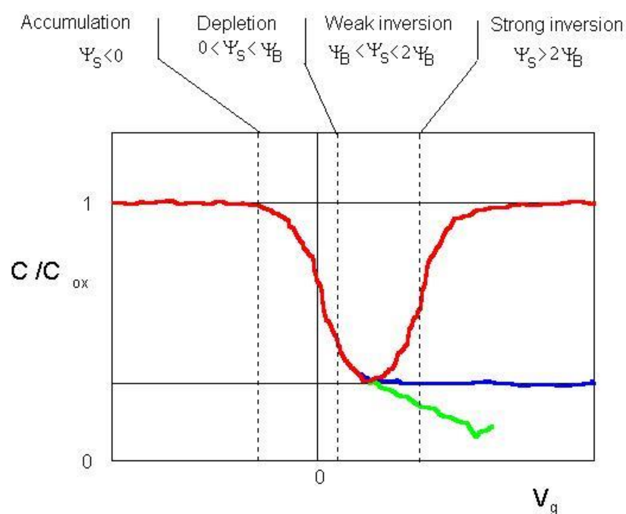


High ac frequency + low ramp rate

Inversion layer can no longer respond, but is still present.

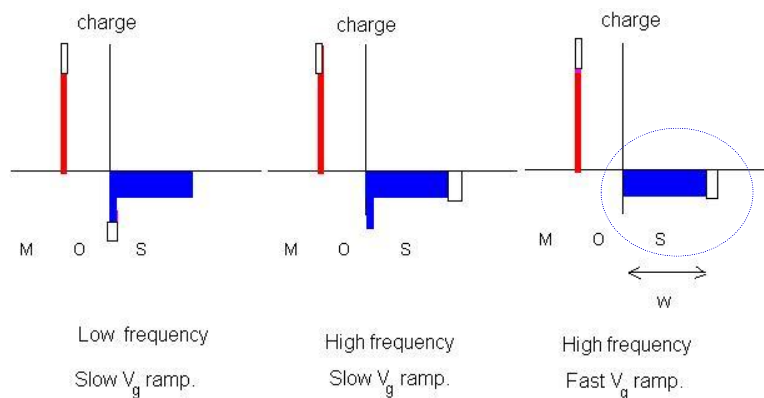
Capacitance due to depletion region in series with oxide.

Experimental dependence of MOS capacitance



Capacitance due to oxide in accumulation, but dips due to additional depletion capacitance in series and stays low without inversion.

Experimental dependence of MOS capacitance

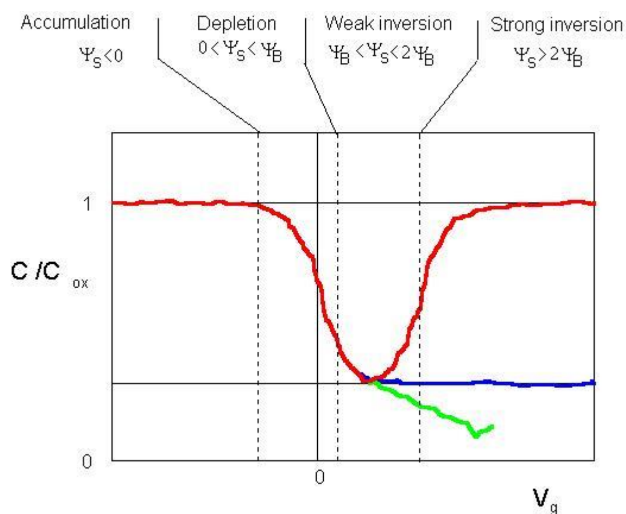


High ac frequency + high ramp rate

Inversion layer does not form.

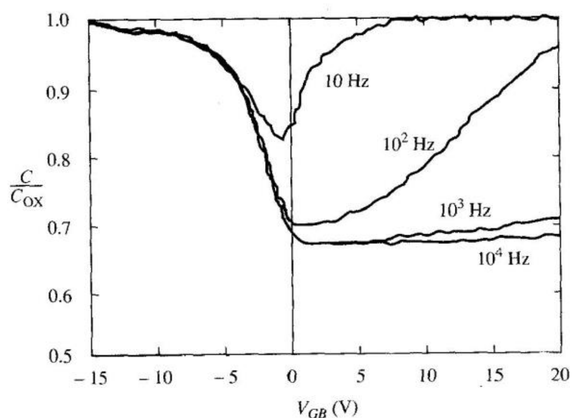
Capacitance due to depletion region in series with oxide Since there is no inversion layer the depletion depth is no longer restricted (deep depletion).

Experimental dependence of MOS capacitance



Capacitance due to oxide in accumulation, but dips due to additional depletion capacitance in series and continues to fall as depletion extends.

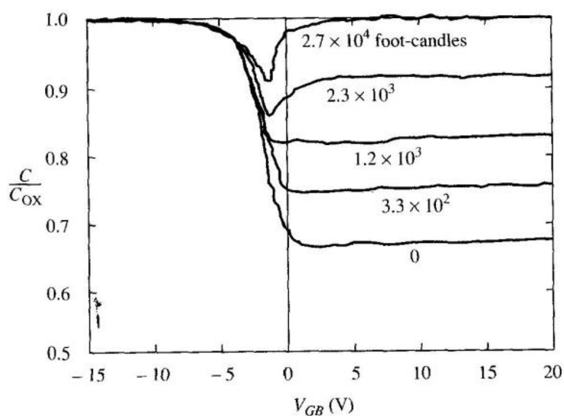
Experimental MOS capacitance



Effect of frequency ……

…… note that 100Hz is already a high frequency as far as the inversion layer is concerned! (NB: “high” or “low” frequencies are materials dependent and, for the same material, vary with the fabrication conditions.)

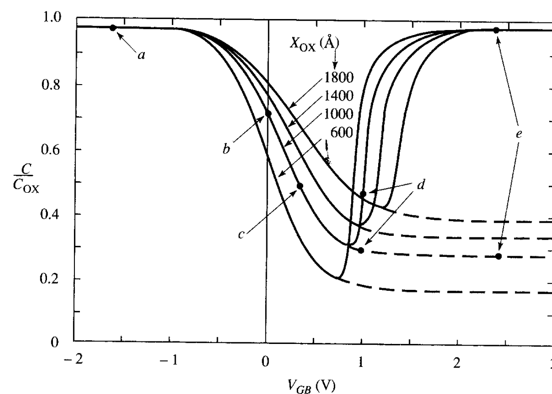
Experimental dependence of MOS capacitance



Effect of illumination ……

…… but if there is a supply of carriers that is faster than generation/recombination then the inversion layer is able to respond again.

Experimental dependence of MOS capacitance



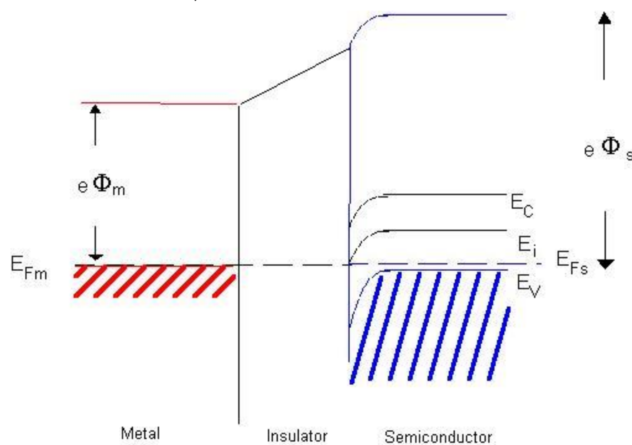
C-V measurements are an important diagnostic tool.

Capacitance depends on oxide thickness, substrate doping, flat band voltage, ……

Non-ideal MOS capacitor

In the ideal MOS capacitor it was assumed that $\Phi_m = \Phi_s$ but in general this is not the case.

For real MOS capacitors in equilibrium, after charge transfer to equalise Fermi levels, we have



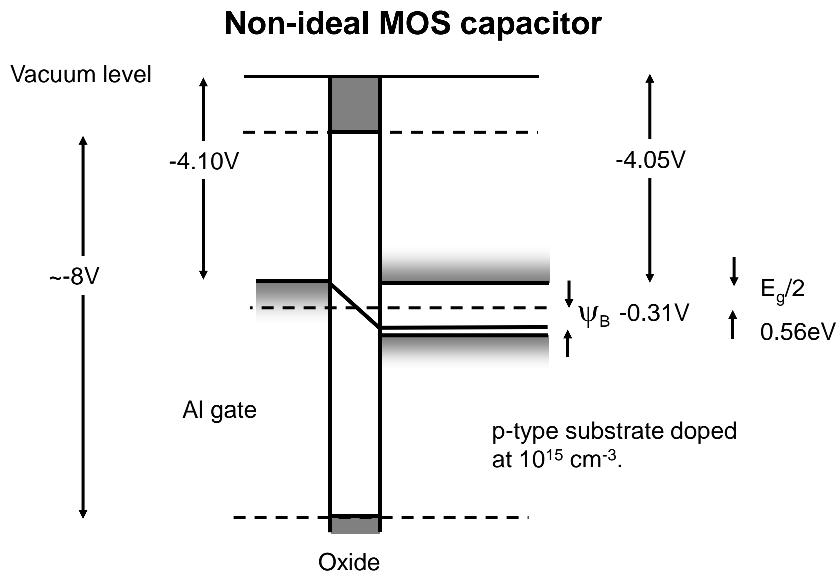
Non-ideal MOS capacitor

To obtain the flat band condition in the non-ideal MOS capacitor, a non-zero voltage $\mathbf{V_{FB}}$ needs to be applied to the gate.

So that the Flat Band gate voltage $\mathbf{V_{FB}}$ is given by

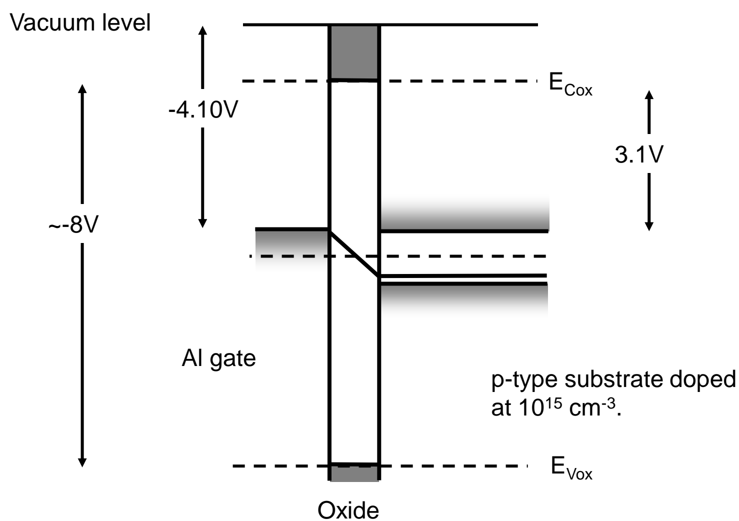
$$V_{FB} = \Phi_m - \Phi_s = \Phi_{ms}$$

Non-ideal MOS capacitor



Originally MOS capacitors were made using Al for the gate, where $\mathbf{\Phi_{ms}}$ is 0.82eV.

Non-ideal MOS capacitor

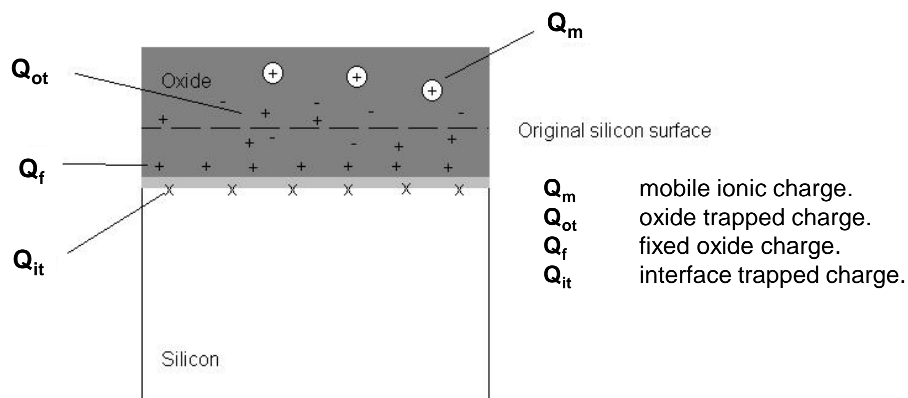


The potential barrier between the conduction bands in silicon and silicon dioxide is only 3.1eV.

Additional fixed and mobile charges

Ideal MOS capacitor assumption only sources of excess charge are at surface of metal and in the semiconductor.

However, as we saw before the oxide has charge ……

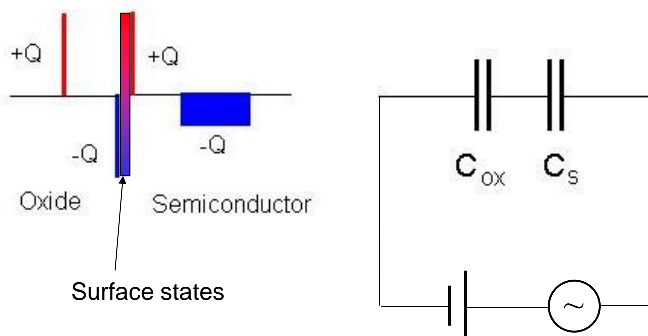


Q_m mobile ionic charge.
Q_{ot} oxide trapped charge.
Q_f fixed oxide charge.
Q_{it} interface trapped charge.

Effect of oxide charge on surface potential

In modern MOS processing the density of interfacial states is of the order $10^9/cm^2$ (comparable to inversion layer density at threshold for $10^{15}/cm^3$ in substrate).

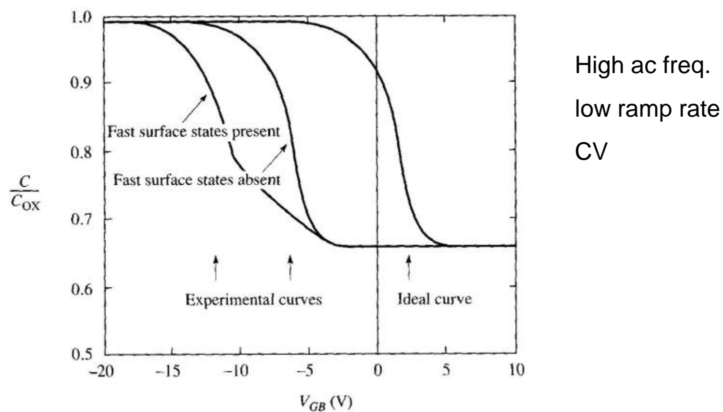
These states act as an electrostatic shield between the gate and the inversion layer reducing the effect of the gate voltage on the surface potential.



Effect of oxide charge on surface potential

The fixed charges $\mathbf{Q_m}$, $\mathbf{Q_{ot}}$, $\mathbf{Q_f}$ and $\mathbf{Q_{it}}$ cause the position of the flat band voltage to shift with respect to zero gate voltage.

In addition, $\mathbf{Q_{it}}$ changes the relationship between the surface potential and the gate voltage.

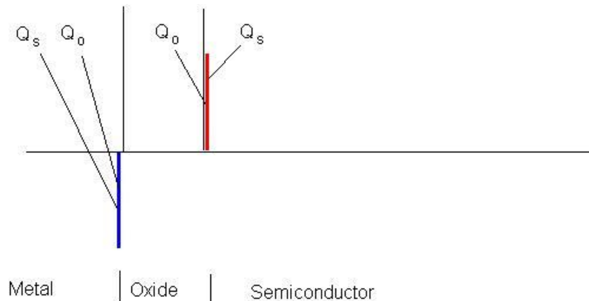


High ac freq.

low ramp rate

CV

Effect of oxide charge on surface potential



To account for oxide charge neglect distribution of charge in oxide.

Assume total fixed charge in the oxide is equivalent to a charge sheet of magnitude $\mathbf{Q_o}$ at the interface.

Similarly, total fixed charge (extra dopant to adjust threshold) in the bulk silicon, near to the oxide-silicon interface, equivalent to a charge sheet of magnitude $\mathbf{Q_s}=\mathbf{Q_I}$ at the interface.

Effect of oxide charge on surface potential

Additional metal-semi. potential difference due to these charges is

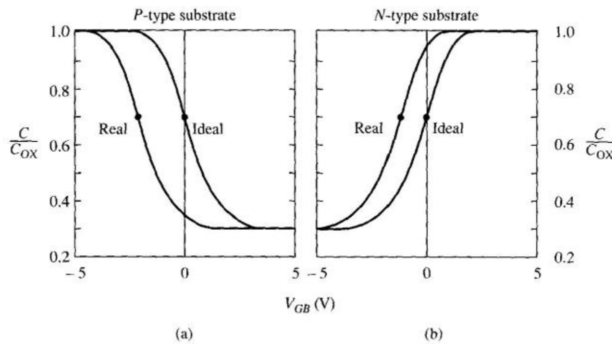
$$-\frac{(Q_o + Q_s)}{C_{ox}} = -\frac{(Q_f + Q_m + Q_{ot} + Q_{it} + Q_I)}{C_{ox}}$$

Including the metal-semiconductor work function electron affinity difference gives a flat band voltage of

$$V_{FB} = \Phi_{ms} - \frac{(Q_o + Q_I)}{C_{ox}}$$

Controlling the magnitude of $\mathbf{Q_I}$ provides a means of controlling $\mathbf{V_T}$, nowadays this is done using ion implantation.

Effect of oxide charge on surface potential

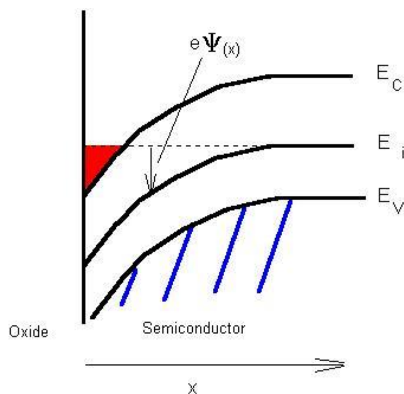


Shifts in the V_{FB} are seen by comparing ideal C-V curves with the experimental curves.

So that the threshold voltage becomes

$$V_T = V_{FB} + 2\Psi_B + \frac{\left(2\varepsilon_0\varepsilon_s 2\Psi_B e N_a\right)^{\frac{1}{2}}}{C_{ox}}$$

Ideal MOS capacitor in inversion



Carrier concentrations

$$n_p = n_i e^{\left[\frac{e\left(\Psi_{(x)} - \Psi_B\right)}{kT}\right]}$$

for electrons in the p-type regions.

$$p_p = n_i e^{\left[\frac{e\left(\Psi_B - \Psi_{(x)}\right)}{kT}\right]}$$

for holes in the p-type regions.

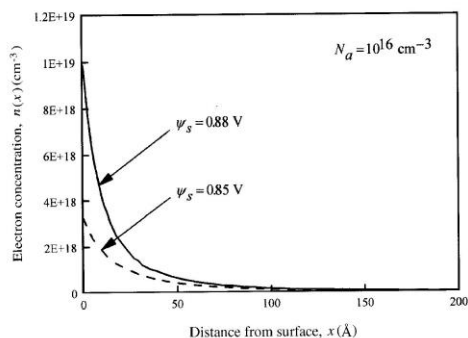
Band diagram close to oxide-silicon interface.

Local potential in the semiconductor $\Psi_{(x)}$ with respect to the bulk material.

Quantum mechanics and threshold voltage

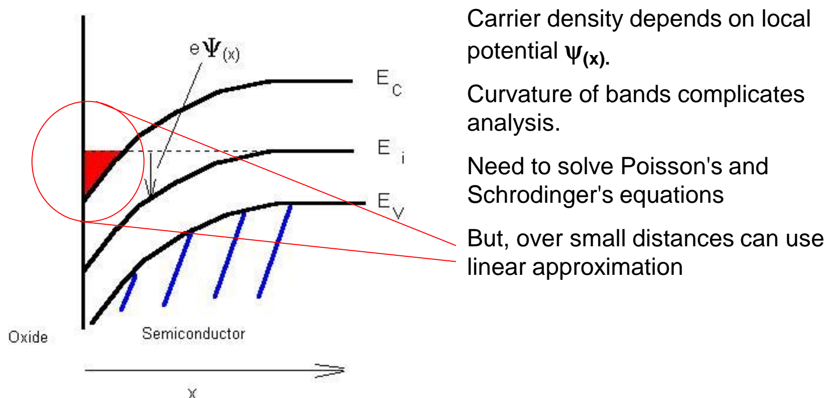
Charge density rises rapidly with surface potential but the width increases only slowly.

In the classical approximation, the carriers in an inversion layer are confined to an ultra-thin region of width comparable to the Fermi wavelength.



This causes quantum corrections to the carrier behaviour.

Quantum mechanics and threshold voltage



Carrier density depends on local potential $\psi_{(x)}$.

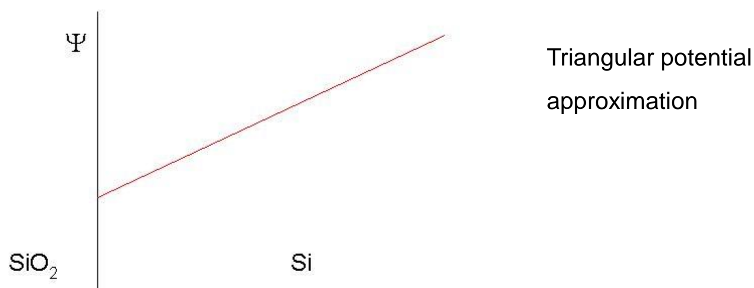
Curvature of bands complicates analysis.

Need to solve Poisson's and Schrodinger's equations

But, over small distances can use linear approximation

Quantum mechanics and threshold voltage

Numerical solution of coupled Poisson's and Schrodinger's equations is given in Stern and Howard, Phys. Rev., **163**, 816, 1967.



Triangular potential approximation

This solution is valid for low inversion charge densities, where curvature due to band bending is weak.

Quantum mechanics and threshold voltage

The boundary conditions are that the electron wave function goes to zero at x=0 and at infinity.

Solution eigenvalues:

$$E_j = \left[\frac{3hqE_s}{4\sqrt{2m_x}} \left(j + \frac{3}{4} \right) \right]^{\frac{2}{3}}$$

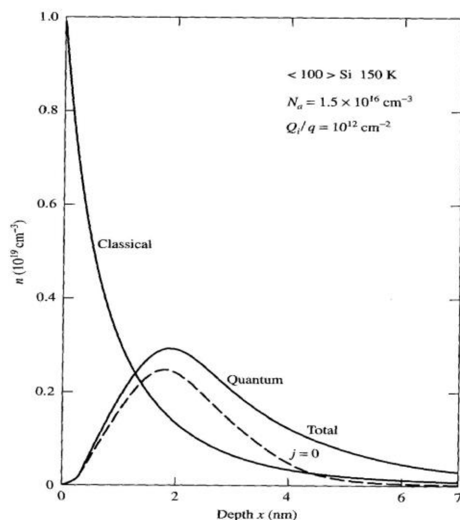
Where j=0,1,2,3..... and $\mathbf{E_s}$ is the electric field at the surface.

For silicon (100) there are two groups of sub-bands or valleys.

	Degeneracy	Effective mass (m_0)
Lower valley	2	0.92
Higher valley	4	0.19

At room temperature several sub-bands in both valleys are occupied (but the majority of electrons in lowest sub-band).

Quantum mechanics and threshold voltage



Peak carrier concentration occurs not at the interface itself but at a short distance away, which is equivalent to an increase in the oxide layer thickness.

This increases the threshold voltage.

Quantum mechanics and threshold voltage

At room temperature and for a surface electric field $\mathbf{E_s}$ in the silicon of <~10^5V/cm, the energy level spacings are smaller than the thermal energy **kT**, so that the classical result holds.

At room temperature and for $\mathbf{E_s}$ >~10^5V/cm, the energy level spacings are larger than the thermal energy **kT**, so that the charge density in the inversion layer is less than the classical prediction.

The latter condition occurs in MOSFET transistors turned hard on so that quantum effects cause an INCREASE in the THRESHOLD VOLTAGE and hence the gate voltage required for a given channel current.

Quantum mechanics and inversion layer thickness

Numerical solutions are required for higher charge densities.

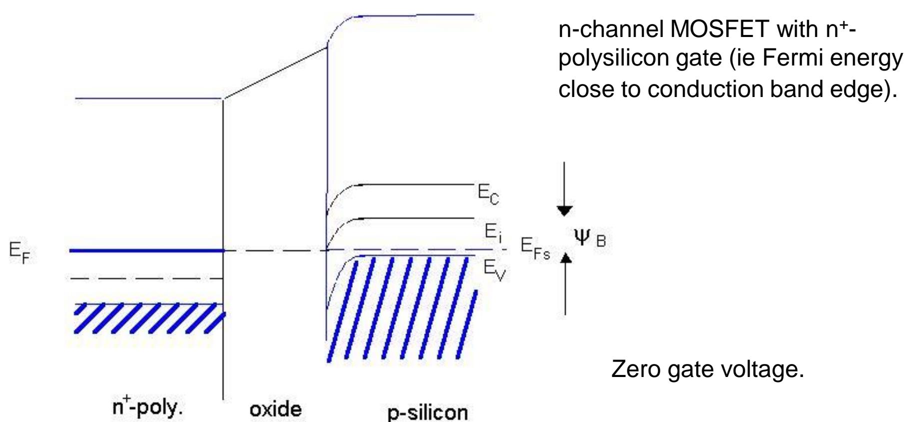
The result is that the quantum mechanical value for the inversion layer depth is about 1nm greater than the classical value.

This is equivalent to 0.3-0.4nm of gate oxide.

The gate oxide thickness is currently around 2-3nm for fully scaled devices and quantum effects add a correction of about 10-20% to the true oxide thickness.

Effect of gate work function on threshold voltage

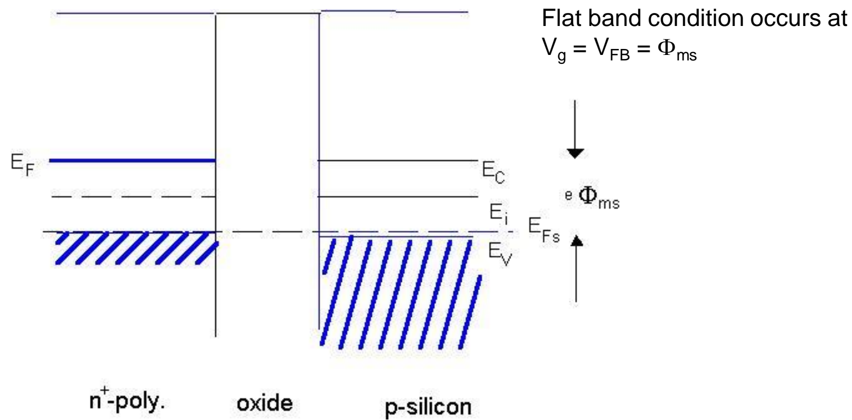
A metal gate is now rarely used in the MOS capacitor structure; processing is greatly simplified if the metal contact is formed from deposited (polycrystalline) silicon.



n-channel MOSFET with n^+-polysilicon gate (ie Fermi energy close to conduction band edge).

Zero gate voltage.

Effect of gate work function on threshold voltage



Flat band condition occurs at $V_g = V_{FB} = \Phi_{ms}$

From diagram

$$\Phi_{ms} = -\frac{E_g}{2e} - \Psi_B = -0.56 - \frac{kT}{e}\ln\left(\frac{N_a}{n_i}\right)$$

Effect of gate work function on threshold voltage

Since
$$V_{FB} = \Phi_{ms} - \frac{(Q_o + Q_I)}{C_{ox}}$$

the correction to $\mathbf{V_T}$ can be included without modification

$$V_T = V_{FB} + 2\Psi_B + \frac{(2\varepsilon_0\varepsilon_s 2\Psi_B e N_a)^{\frac{1}{2}}}{C_{ox}}$$

Similar corrections apply for p-channel devices
with appropriate change of sign.

Effect of gate polysilicon depletion

The deposited (polycrystalline) gate silicon is usually highly doped to give a high conductivity.

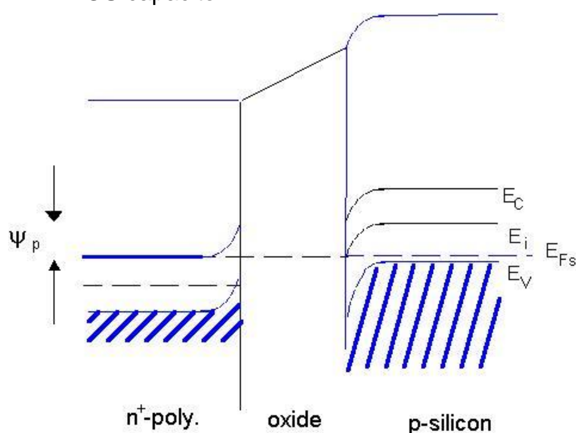
However, if the gate is not doped sufficiently (the maximum doping density is limited by solid solubility effects) it is necessary to take into account the depletion of the gate electrode, which results in an additional capacitance in series with the oxide capacitance.

The effect of this shows up in the low frequency CV characteristics.

Effect of gate polysilicon depletion

A positive voltage applied to the n+ polysilicon gate causes band bending of ψ_p at the polysilicon-oxide interface, which results in depletion of the gate.

This requires an additional correction to the flat band voltage of a non-ideal MOS capacitor.



Worked example

Find the threshold voltage for an n-channel MOSFET with an n^+ gate if $t_{ox} = 0.1\mu m$, $N_a = 3x10^{15}$ cm^{-3}, gate doping $N_D=10^{20}$ cm^{-3}, and if the positively charged ion density at the oxide-silicon interface is 10^{10} cm^{-2}. The potential due to the substrate doping is

$$\Psi_{B(sub)} = \frac{kT}{e}\ln\left(\frac{N_a}{n_i}\right) = 0.026 \times \ln(3\times10^5) = 0.328\,V$$

The potential due to the gate doping is

$$\Psi_{B(gate)} = -\frac{kT}{e}\ln\left(\frac{N_D}{n_i}\right) = -0.599\,V$$

Worked example

The potential difference between the gate and the substrate is

$$\Psi_{B(gate)} - \Psi_{B(sub)} = -0.599 - 0.327 = -0.926\,V$$

The oxide capacitance is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\varepsilon_0}{t_{ox}} = 3.45\times10^{-4}\,Fm^{-2}$$

Worked example

The charge in the depletion layer is $Q = \left(\Psi_s 2\varepsilon_o \varepsilon_s e N_a\right)^{\frac{1}{2}}$

and the surface potential at threshold is $\Psi_s = 2\Psi_B = 2\Psi_{B(sub)}$

So that the depletion layer charge is

$$Q_{dep} = -\left[(2\Psi_B) 2\varepsilon_o \varepsilon_s e N_a\right]^{\frac{1}{2}} = -2.51 \times 10^{-4}\, Cm^{-2}$$

for the negatively charged acceptors.

The potential difference across the oxide layer due to this charge is

$$V = \frac{Q}{C_{ox}} = 0.728\, V$$

Worked example

Finally, the potential difference across the oxide layer due to the positive oxide-silicon interface charge is

$$V = -\frac{Q_I}{C_{ox}} = -0.046\, V$$

Summing all of the contributions to the potential difference across the oxide at threshold gives

$$V_T = -0.926 - 0.046 + 2 \times 0.328 + 0.728 = 0.412\, V$$