UNIVERSITY OF CAMBRIDGE

Solid State Devices

4B6

Lecture 1 – Introduction

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Lent 2016

Course outline

Introduction (1L) — **Today's subject**

MOS capacitors (2L)

MOSFET (2L)

Thin-film transistor (TFT) technology (1L)

Nonvolatile memories:

Ferroelectric RAM (FRAM) (2L)

Nonvolatile memories:

Magnetic RAM (MRAM) (2L)

Displays (LCD, DLP and LCOS) (1L)

Chemical and biological sensors (2L) — **by Dr M Y Ho, 10-121 (tbc)**

Microelectronics – Traditions

Trends:

- Smaller geometries;
- Higher speed;
- Higher device density:

  Volatile memories (DRAMs, SRAMs)

  Non-volatile memories (Flash memories, FRAMs, MRAMs)
- Lower power (!)

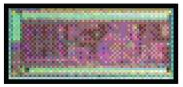
Conventional concepts + Technology progress ➔ 0.018μm

Completely new concepts needed when going further:

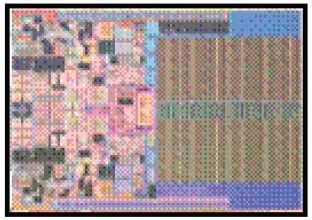
- Single electron transistor;
- Quantum dots / Single molecules / ... ...

Microelectronics – 45nm microprocessor products

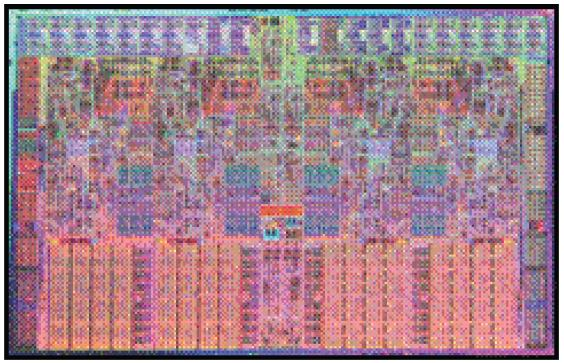
Single Core

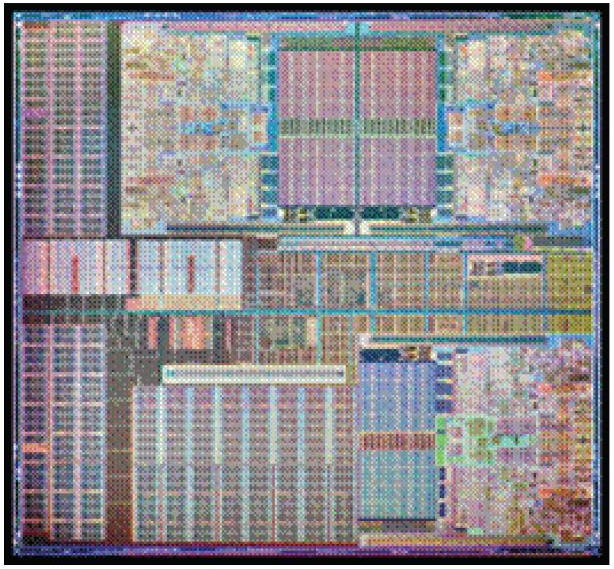


Dual Core

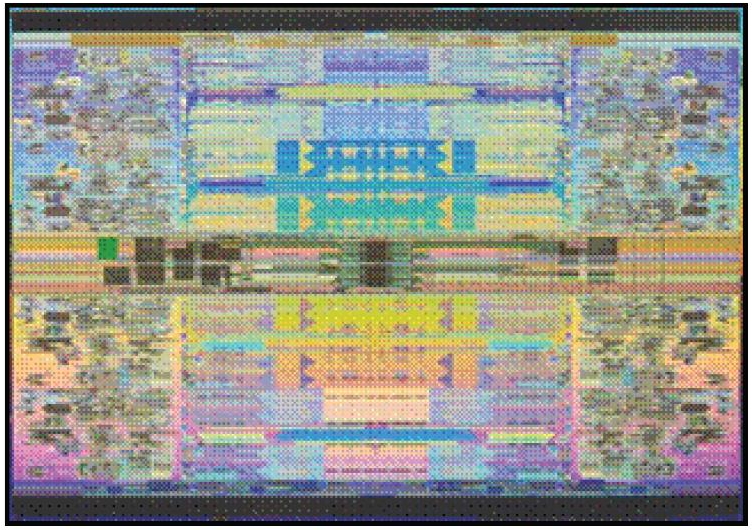


Quad Core





6 Core



8 Core

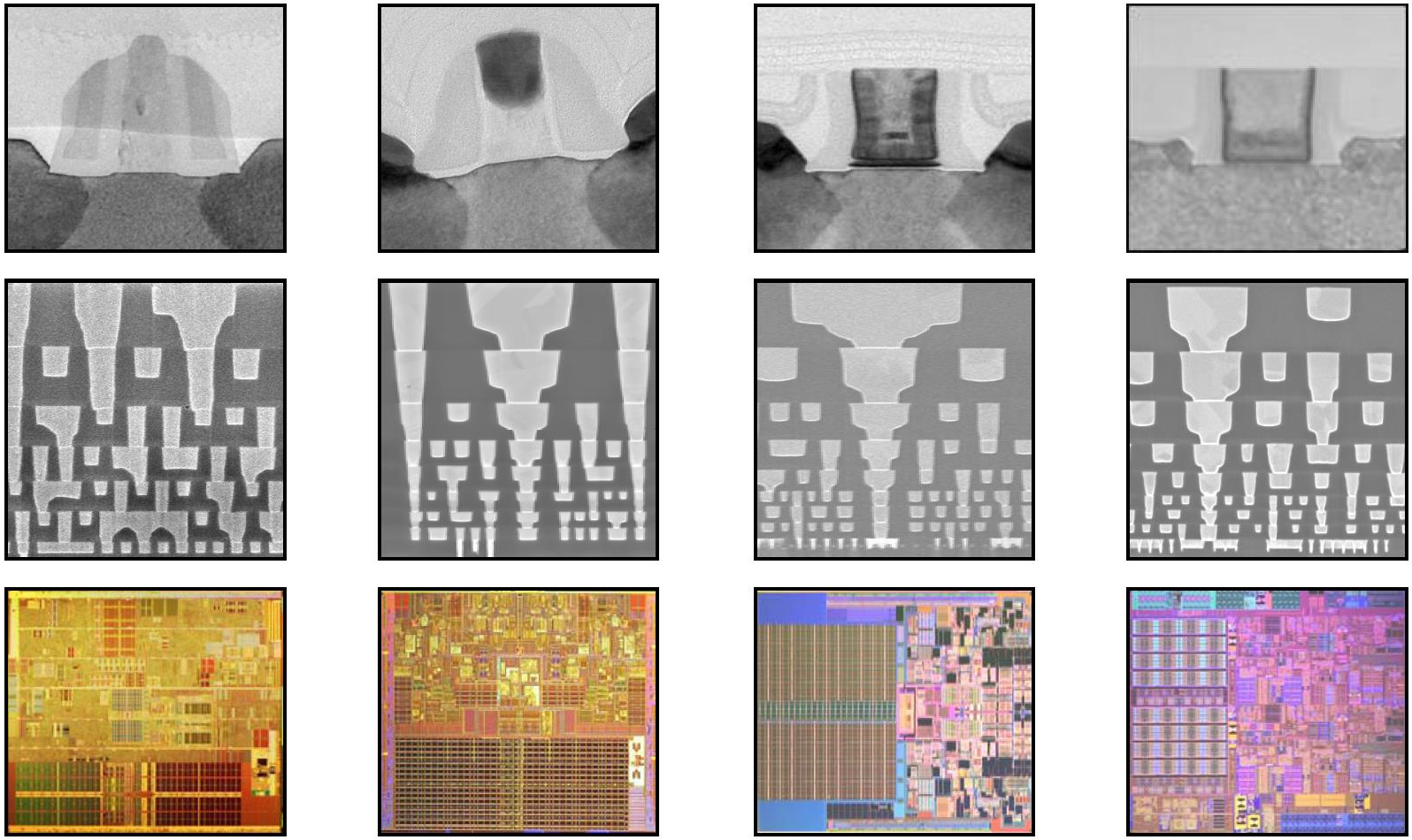
>200 million 45 nm CPUs shipped to date

2009

intel

Microelectronics – Transistor channel length

90 nm	65 nm	45 nm	32 nm
2003	2005	2007	2009



2009

Microelectronics – Moore's law

Based on silicon MOSFET:

New technology generation every 2 years:

- 2x transistors per die
- 0.5x cost per transistor
- 2x processor speed

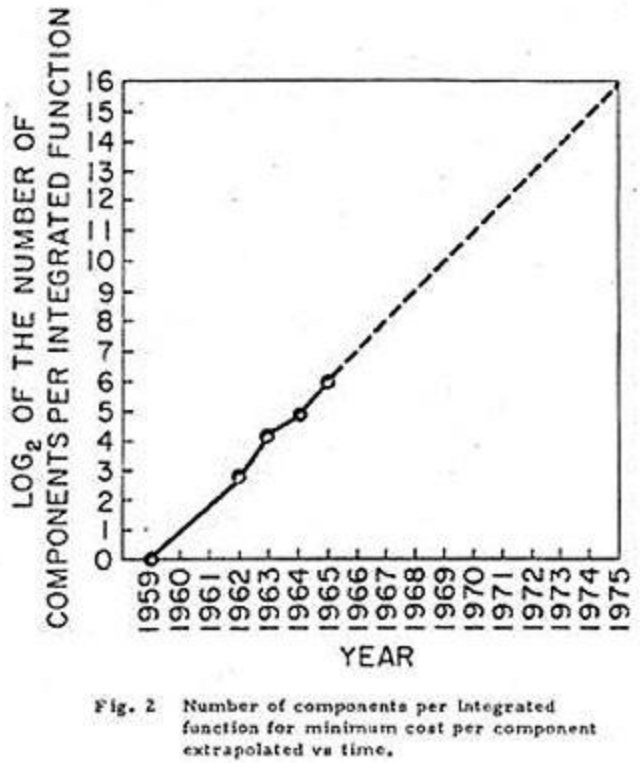
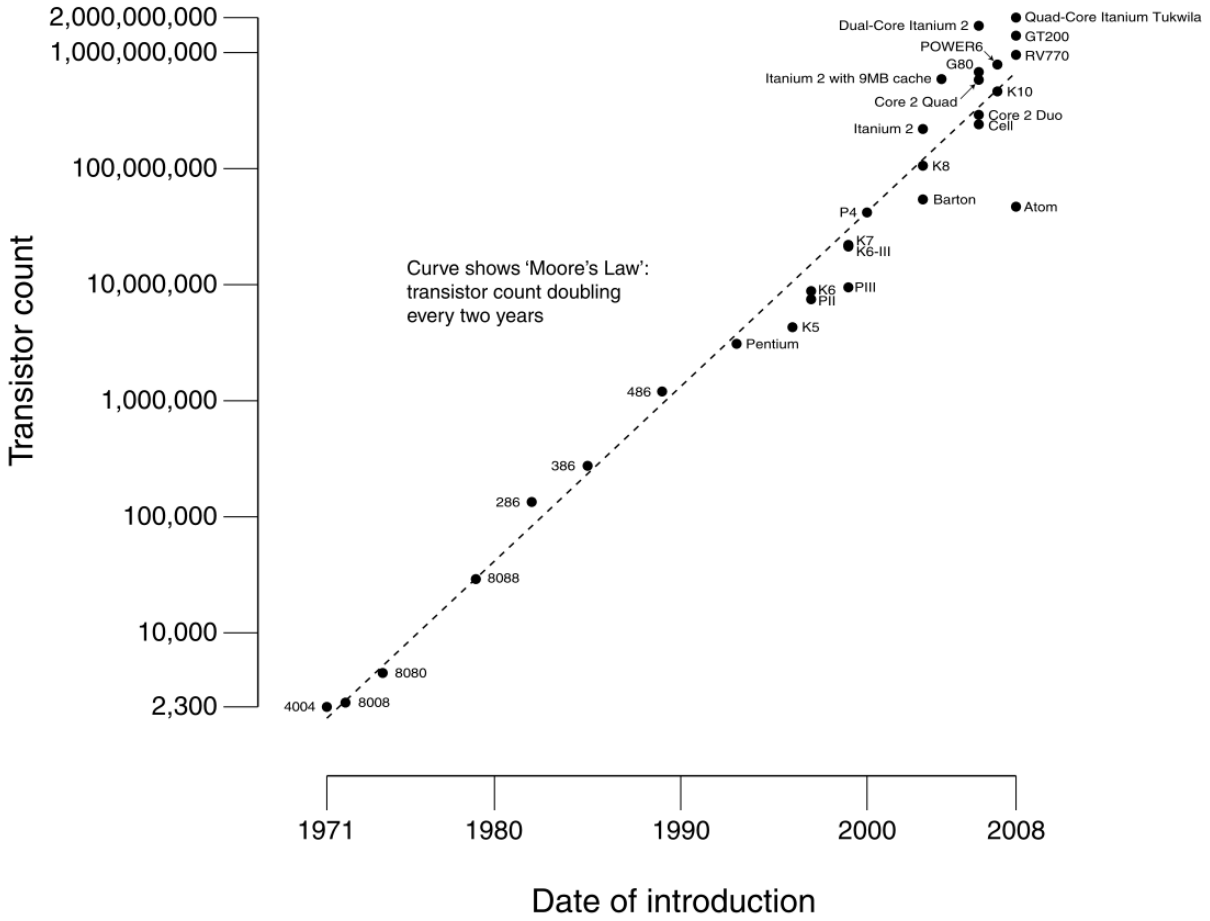


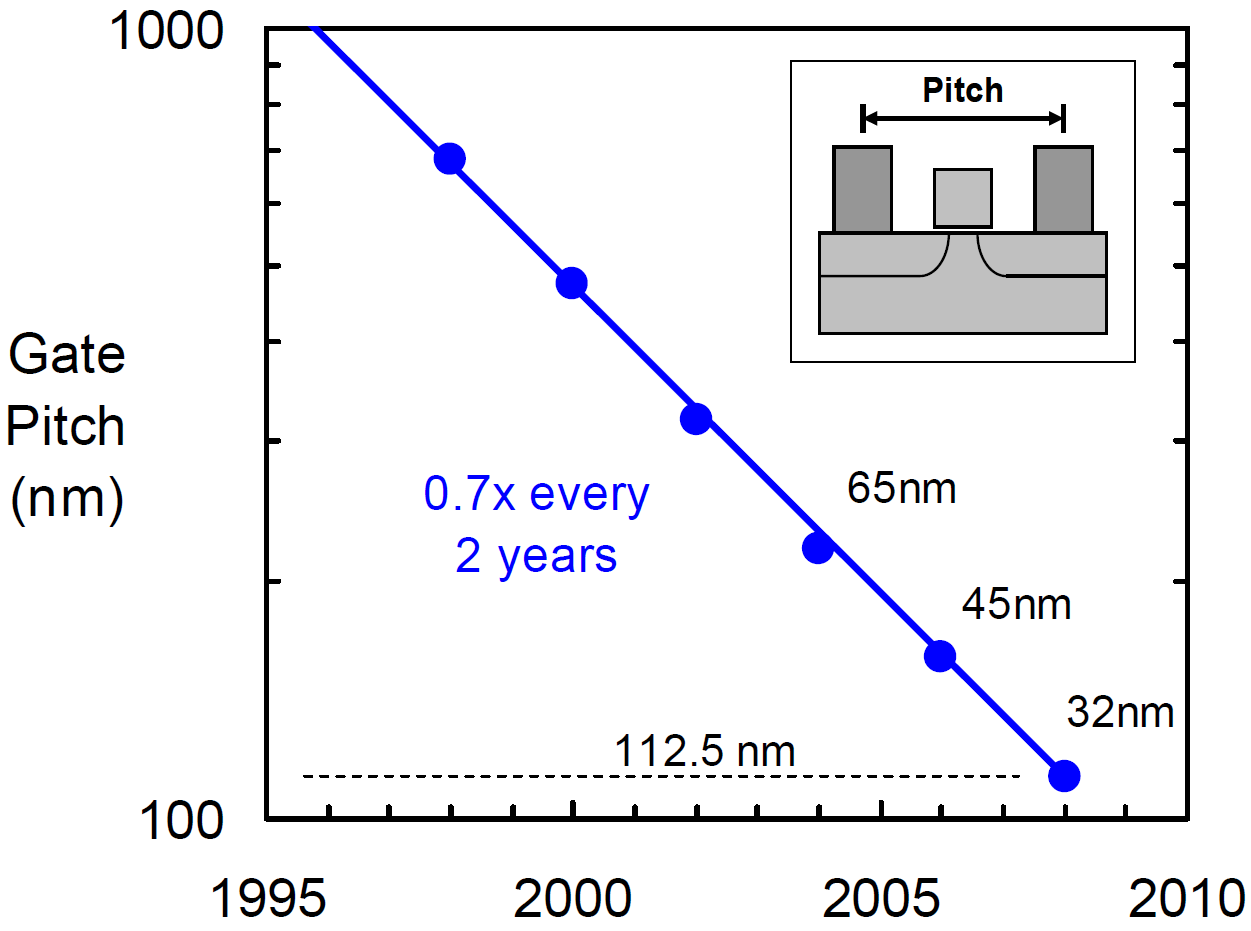
Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.



Gordon E. Moore, Electronics, Vol. 38, No. 8 (1965).

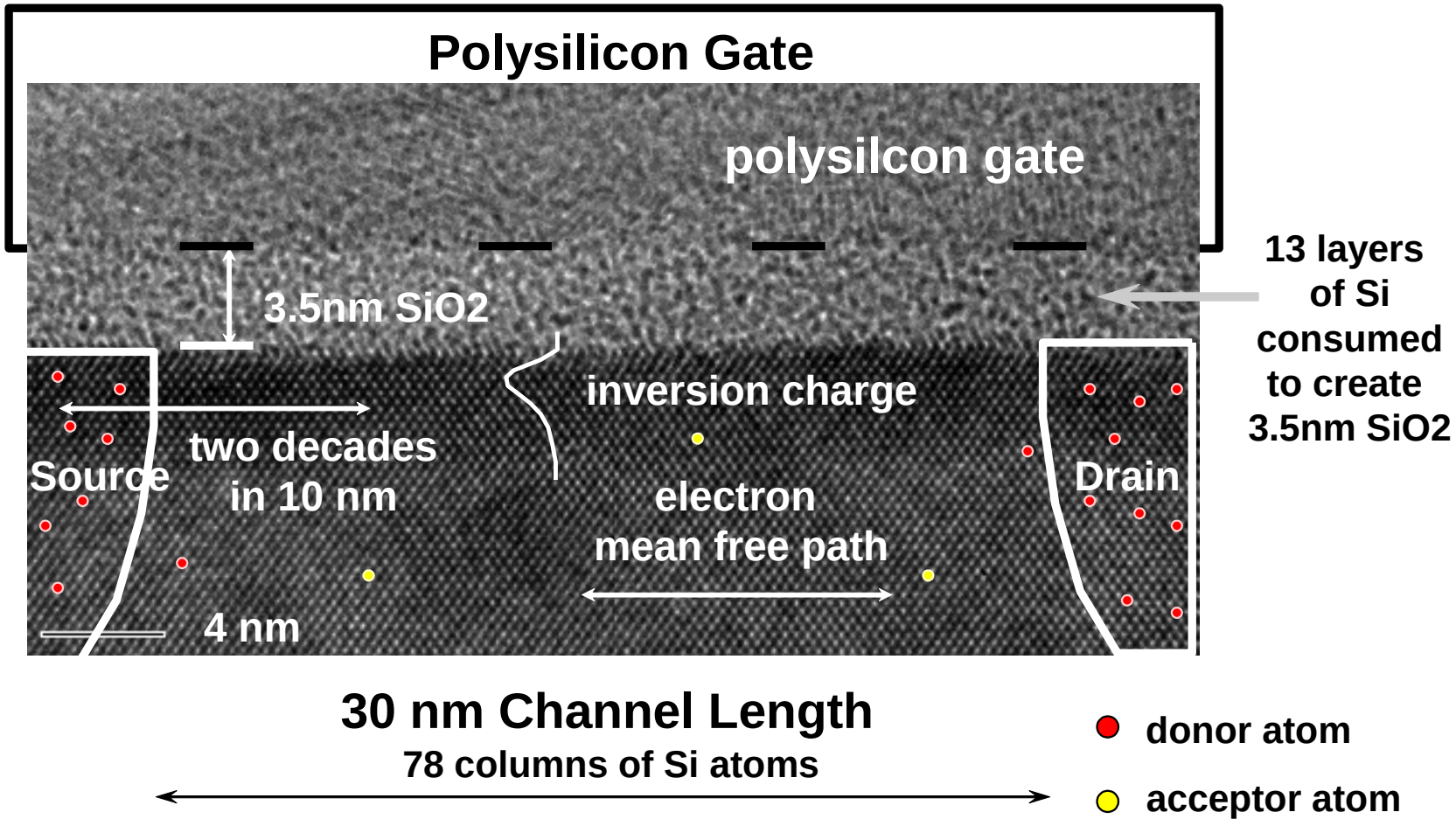
Microelectronics – Transistor gate pitch

0.7x Gate pitch ⟷ 0.5x Transistor size ⟷ 2x Number of transistors

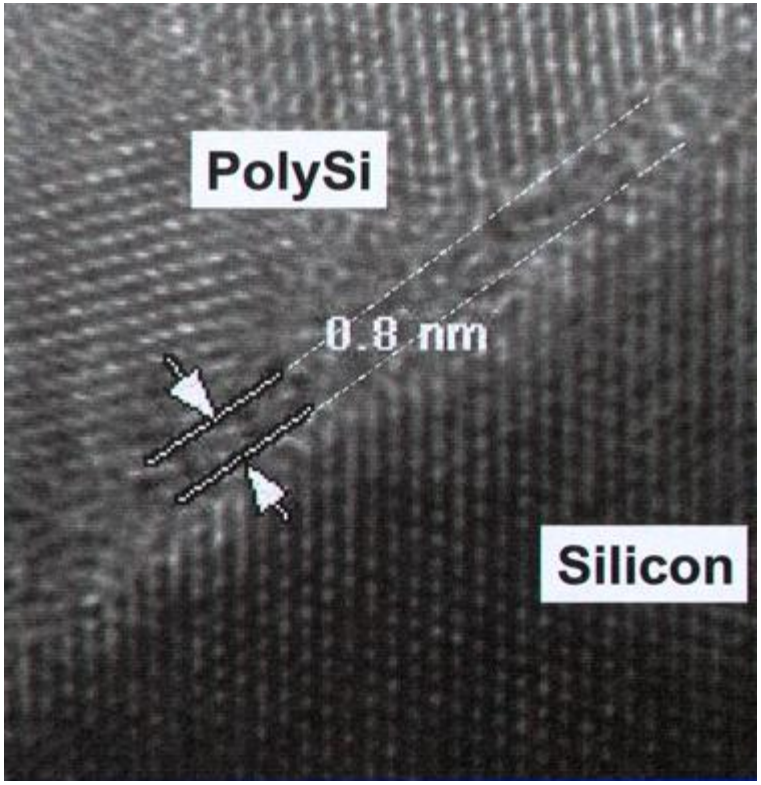


2009

Microelectronics – HRTEM of a 30nm channel

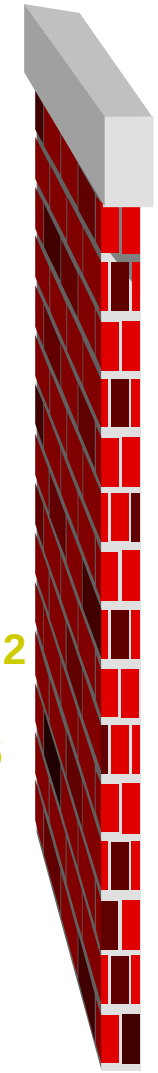


Microelectronics – 0.8nm gate oxide



Microelectronics – Technology “Brick Wall”(?)

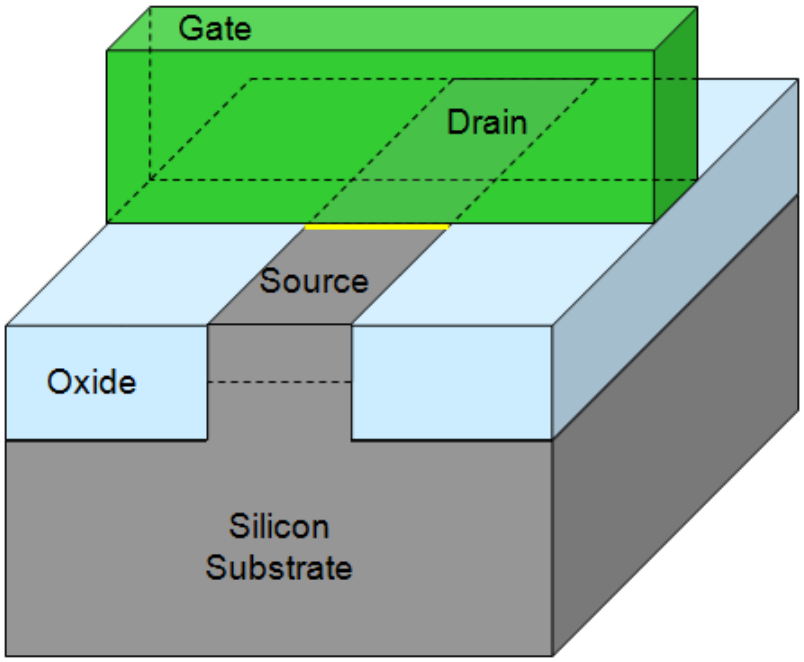
Year of Production:	1999	2002	2005	2008	2011	2014
DRAM Half-Pitch [nm]:	180	130	100	70	50	35
Overlay Accuracy [nm]:	65	45	35	25	20	15
MPU Gate Length [nm]:	140	85-90	65	45	30-32	20-22
CD Control [nm]:	14	9	6	4	3	2
T_{OX} (equivalent) [nm]:	1.9-2.5	1.5-1.9	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6
Junction Depth [nm]:	42-70	25-43	20-33	16-26	11-19	8-13
Metal Cladding [nm]:	17	13	10	0	0	0
Inter-Metal Dielectric K:	3.5-4.0	2.7-3.5	1.6-2.2	1.5	<1.5	<1.5



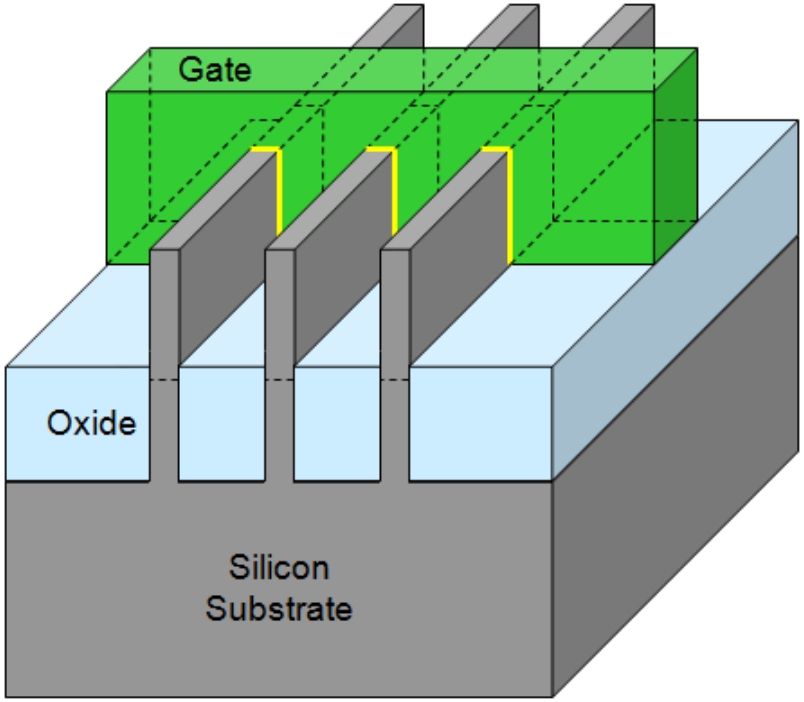
Based on Robert Doering (Texas Instruments)

Microelectronics – Tri-Gate / FinFET

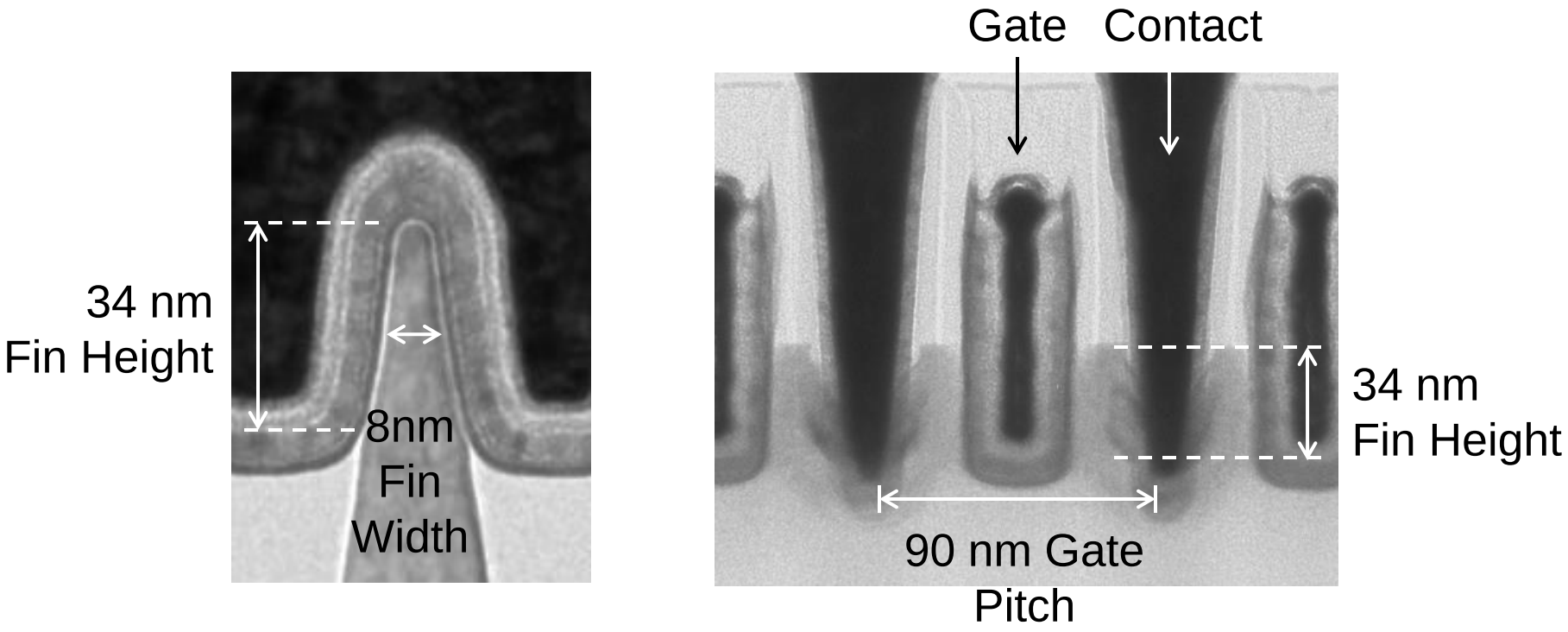
Planar Transistor



FinFET

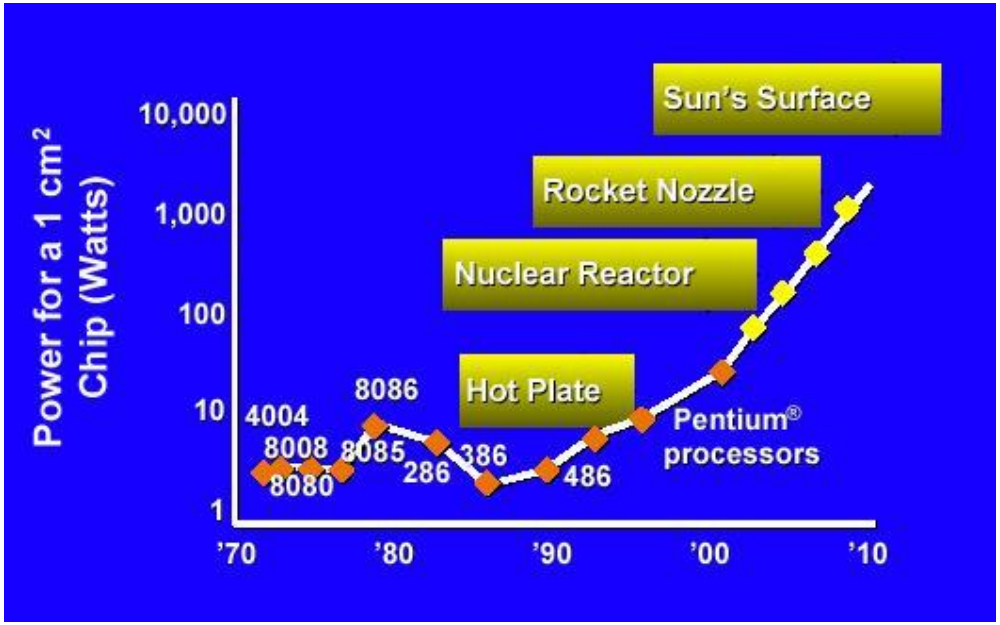


Microelectronics – Tri-Gate / FinFET



- Intel's 22nm Tri-Gate/FinFETs
  - Key manufacturing challenges are control of Fin Height and Fin Width
  - 3-D Tri-Gate structure provides higher drive current in given footprint

Microelectronics – Power dissipation in VLSI

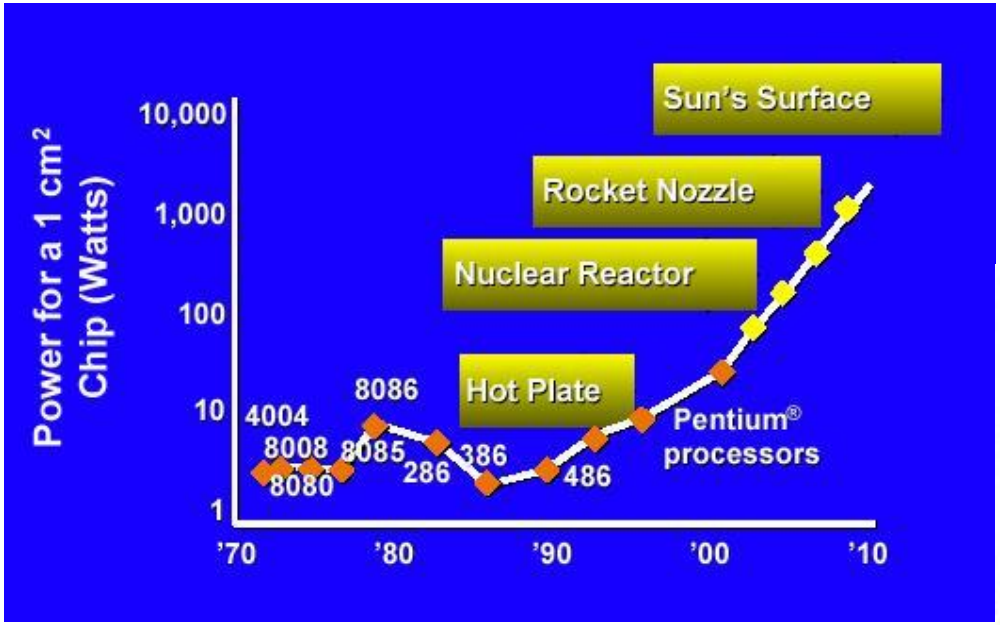


Power density no longer maintained in deep sub-micron MOSFETs.

Recent increases are exponential.

www.intel.com/research/silicon

Microelectronics – Power dissipation in VLSI



One solution to the problem of chip overheating!

www.vapochill.com

Course principles

This course is all about the microelectronics devices ... ...

and the principle for operation and their applications.

The history of the microelectronics industry has followed Moore's Law over the last 40 years or so ... ...

But ... ...

there are many semiconductors with better properties than silicon;

there are many transistor types with better properties than the MOSFET.

The reasons for the dominance of the silicon MOSFET have a basis in PHYSICS ... ... and that is what this course is all about.

Course principles – Choice of transistor type

First successful device action was achieved in bipolar transistors

MOSFETs took much longer to get to work, as carrier transport is near to surface, where scattering and trapping occurs:

- transconductance much better in bipolar, rather than MOSFET, transistors;
- speed much better in bipolar, rather than MOSFET, transistors;
- MOSFETs easily damaged by static discharge.

There does not seem to be much in favour of MOSFETs ... ...

Course principles – Use of transistors as switch

But most transistors are just used as a switch!

What is important about a switch is:

how well it turns ON and OFF;

needs to do this faster than circuit speed, but no advantage to extra speed;

power dissipation;

circuit density.

Course principles – Use of switches to perform logic

Combinations of switches can be used to perform logic.

Very large numbers of switches results in very complex logic operations:

Intel Quad Core now has 2 billion transistors!

Operating them at high speed gives impressive computing power.

Course principles – Use of CMOS to perform logic

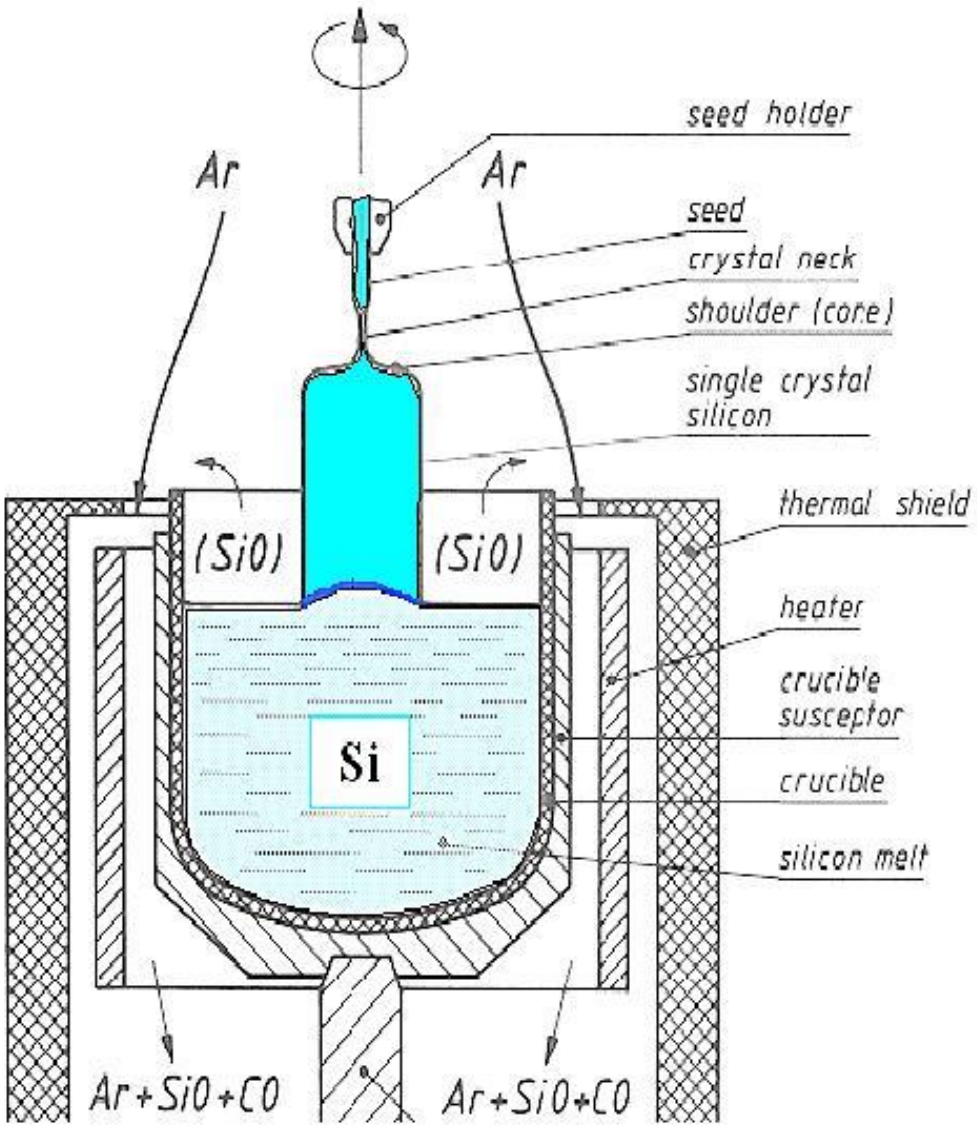
Combinations of complimentary transistors (p- and n-channel) are particularly advantageous.

Static power dissipation can be reduced to near zero!

Very important if you have millions / billions doing nothing!

But still need to take care of dynamic power.

Semiconductor crystal growth

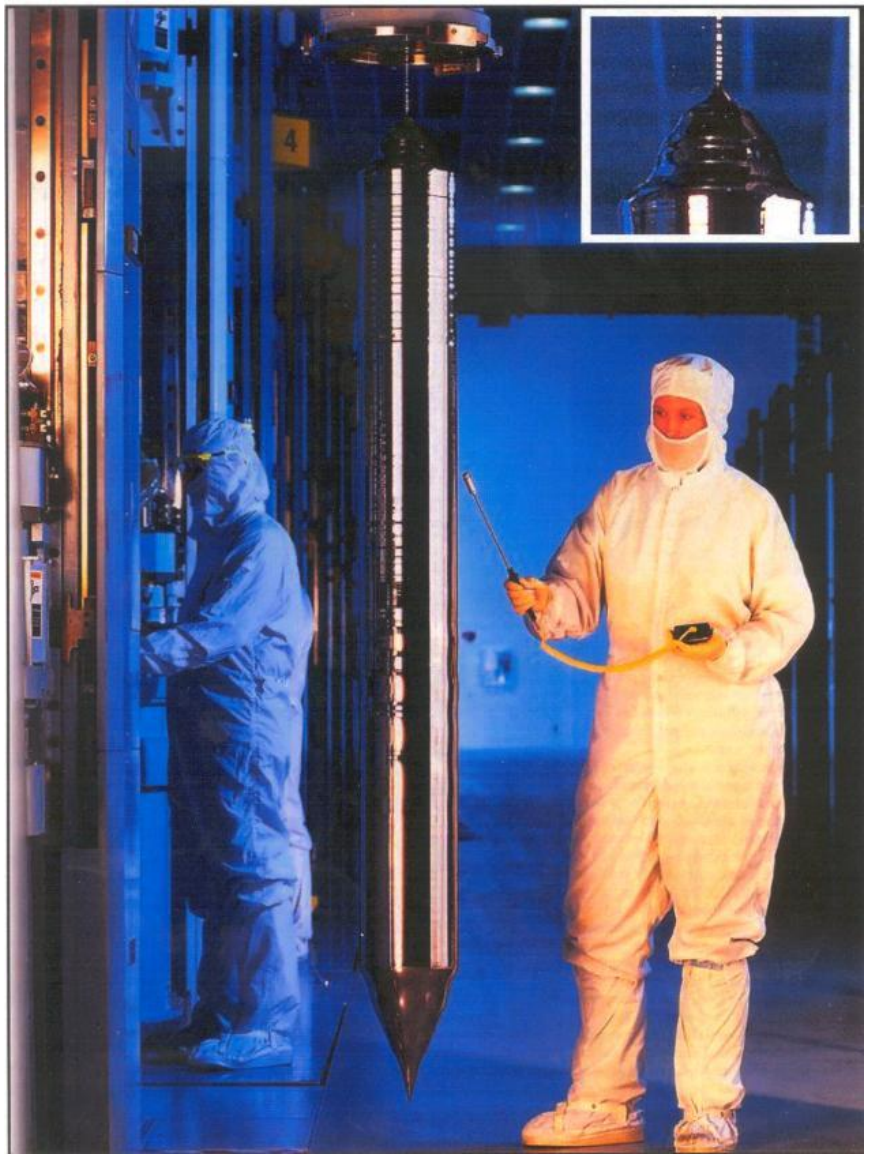


Czochralski method

Requirements:

- control of dT/dz at crystal-liquid interface;
- inert atmosphere.

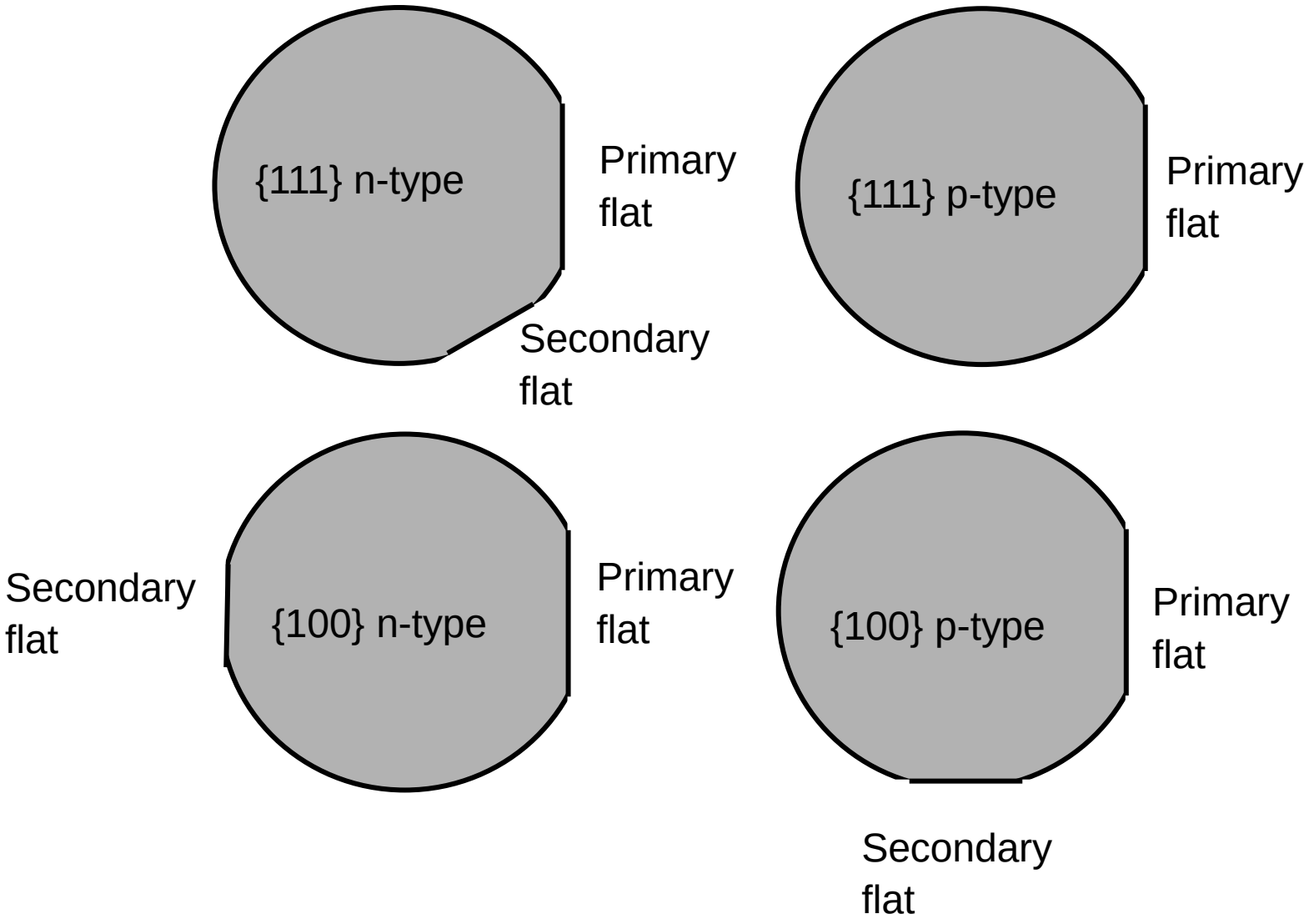
Semiconductor crystal growth



Production of a large silicon ingot:

- Clean processing;
- Very high strength of single crystal silicon;
- Then sliced into wafers with precise orientation.

Wafer orientation



Uses of dielectrics in microfabrication

Both deposited and grown dielectrics are used in microfabrication.

Gate dielectric – thin, highest $E_{breakdown}$, lowest density of states in bandgap.

Ideal dielectric has no states in bandgap and infinite $E_{breakdown}$.

Silicon dioxide is the most important.

Used as gate dielectric in silicon MOSFETs (almost perfect insulator with a resistivity > $10^{16}\Omega$cm).

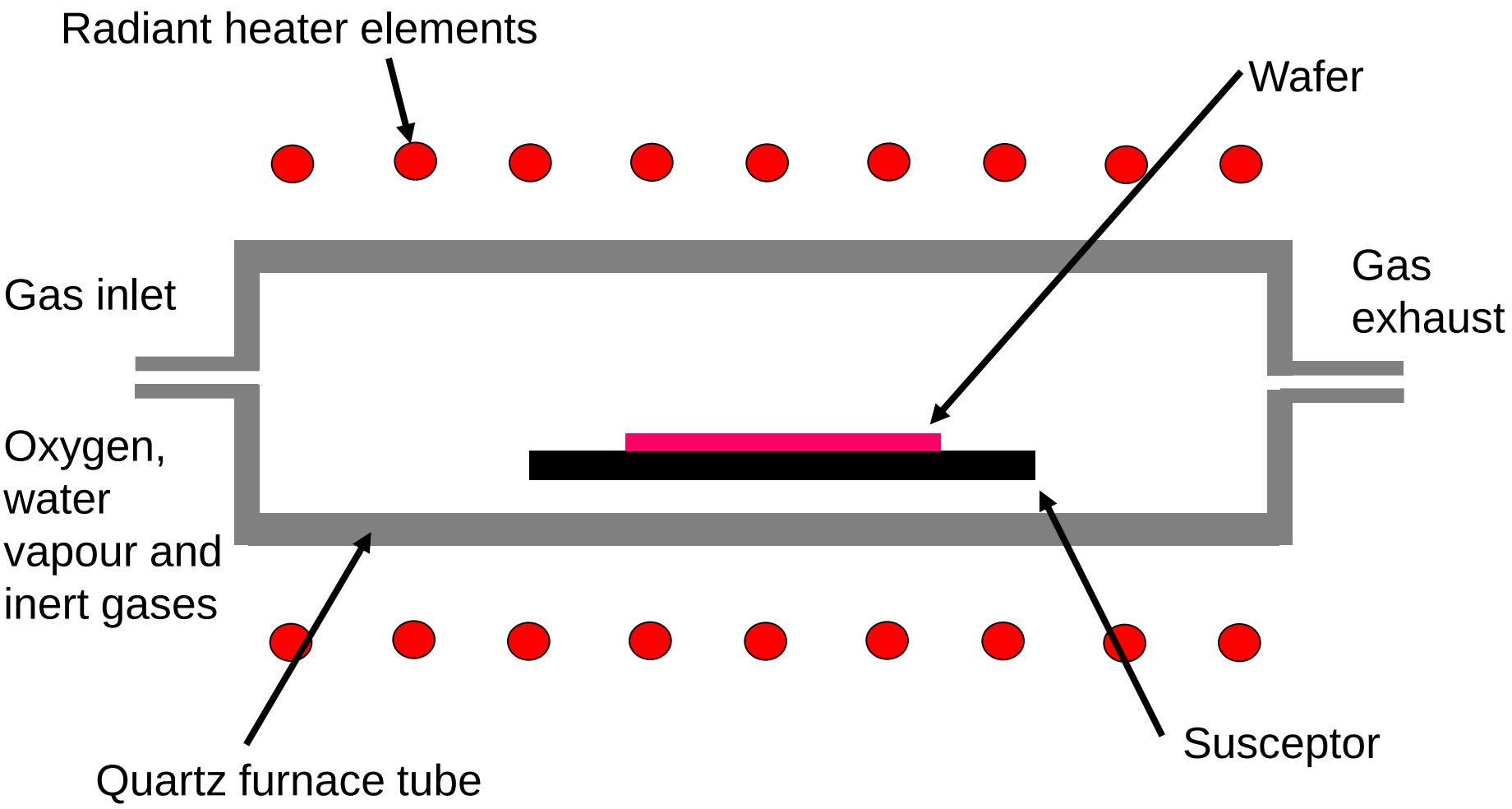
Single most important reason for success of silicon MOSFET technology.

Uses of dielectrics in microfabrication

Gate dielectric –

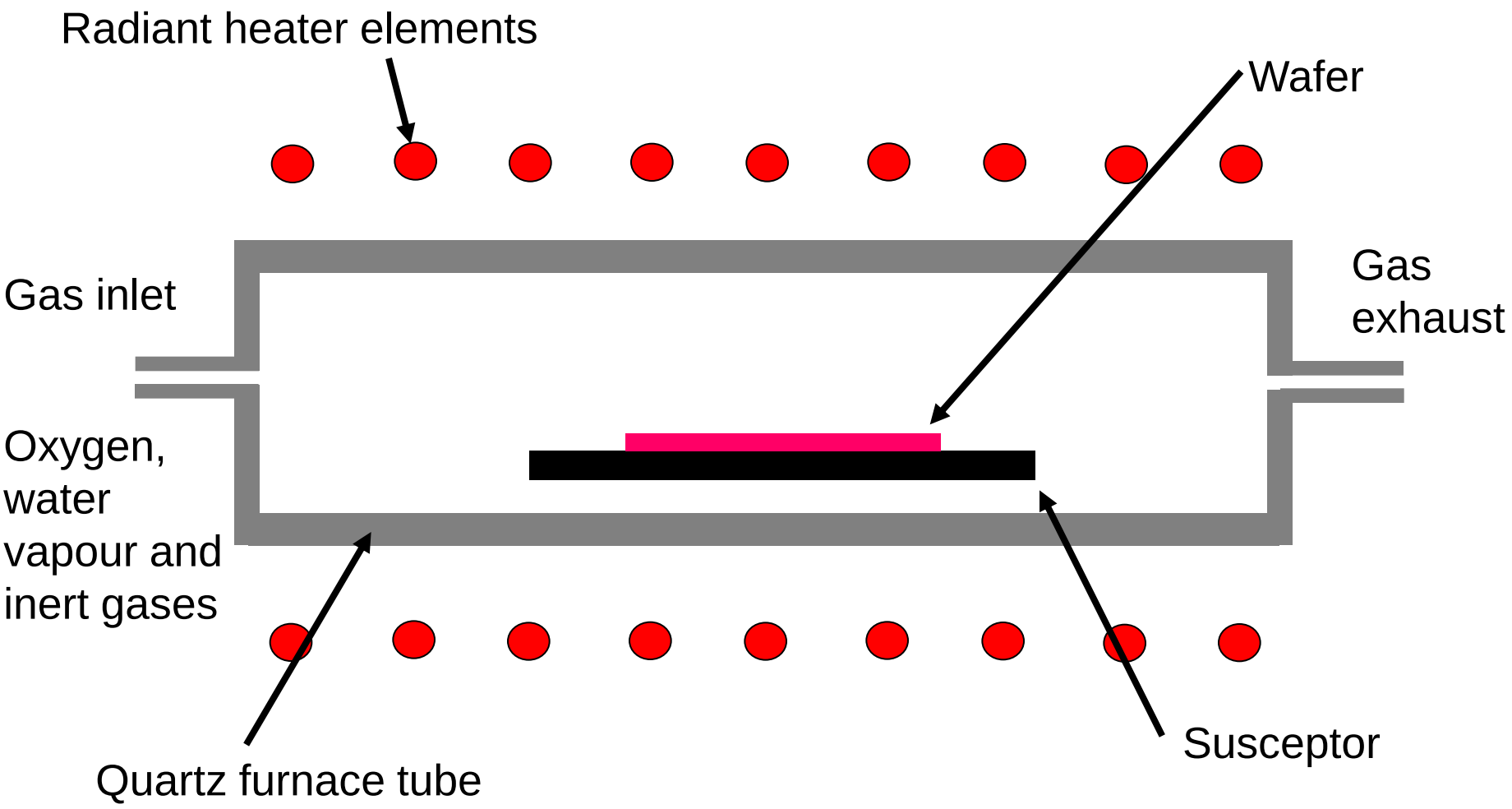
- grown by thermal oxidation
- consumes silicon from substrate
- only oxygen transported from outside

Thermal oxidation



Silicon dioxide is usually grown by thermal oxidation (heating to temperatures above 900C in an oxidising atmosphere).

Thermal oxidation



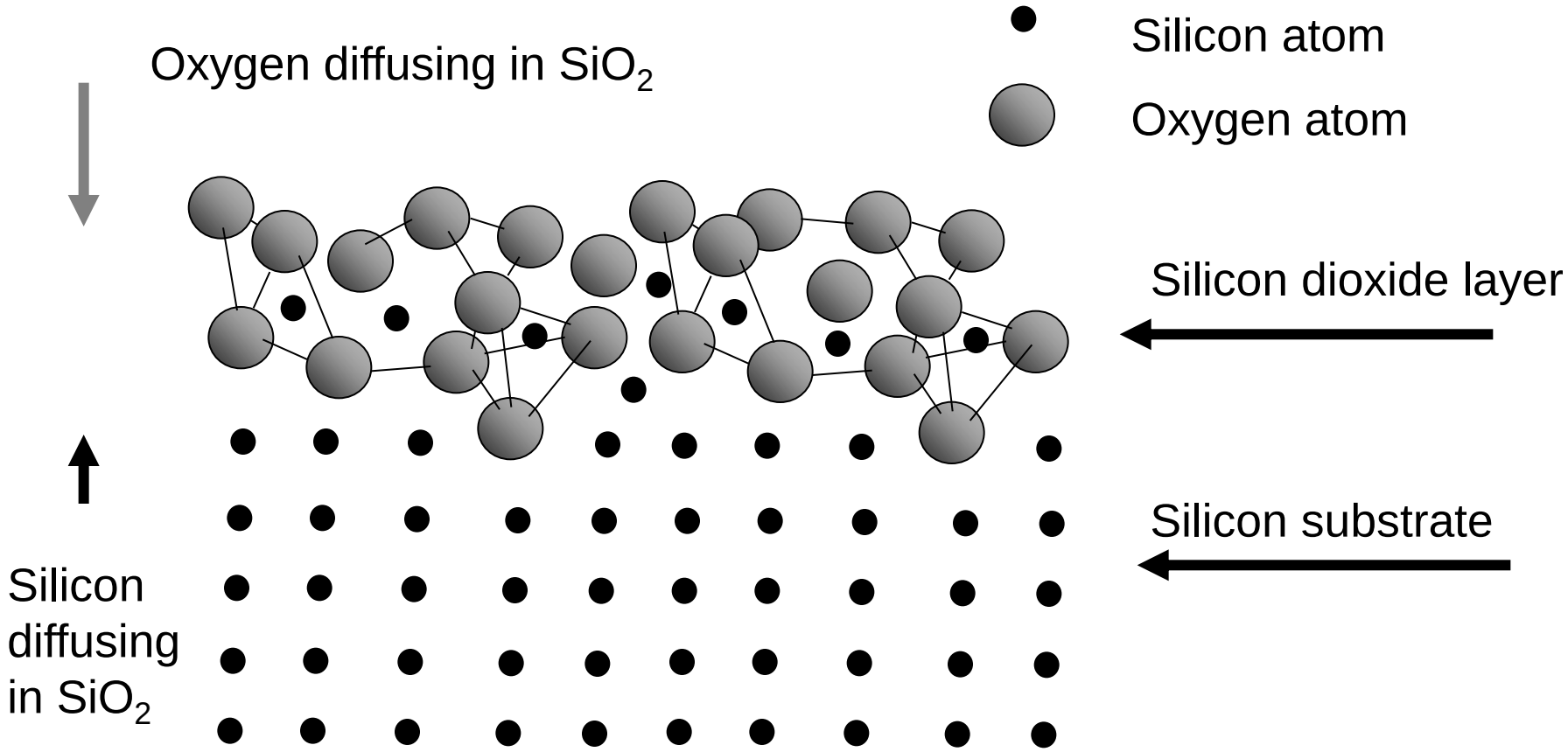
Different apparatus to that used for CVD to avoid autodoping problems.

Oxidation furnace

Batches of wafers processed at same time.

Thermal oxidation

Thermal oxidation takes place by oxygen (water vapour) diffusing through the silicon dioxide and reacting with silicon from the underlying substrate forming amorphous silicon dioxide (open structure).



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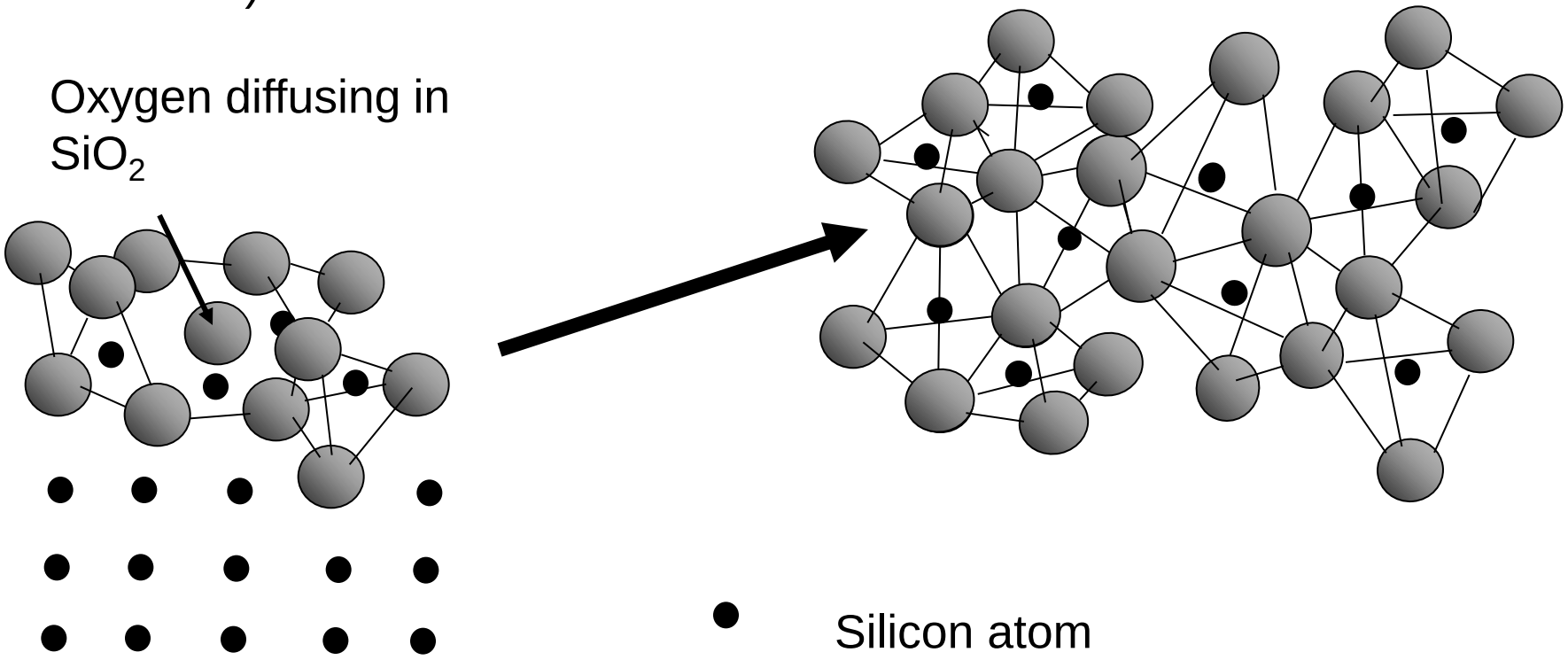
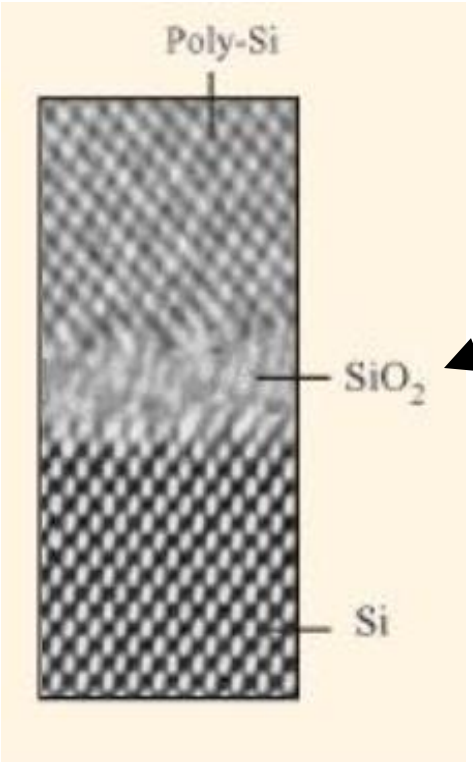
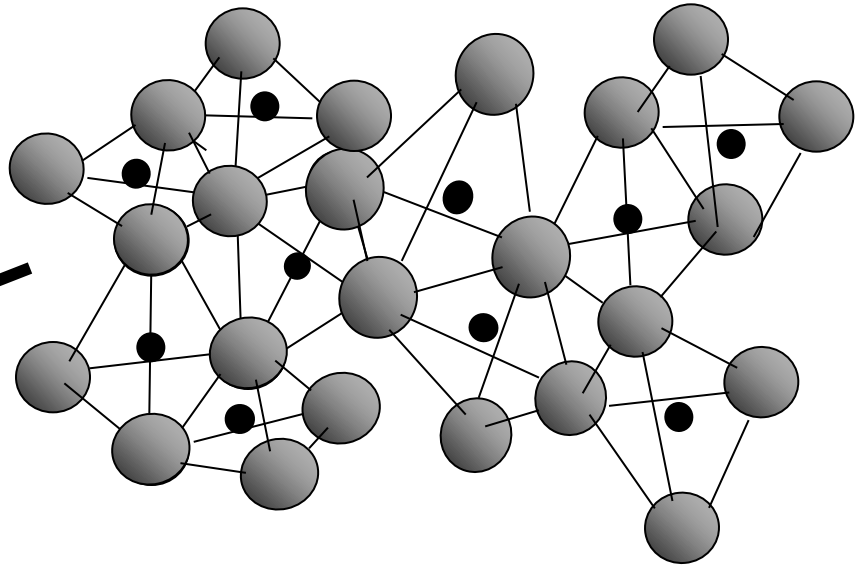


Thermal oxidation

The growth of new oxide is protected by the overlying dielectric and so is very clean.



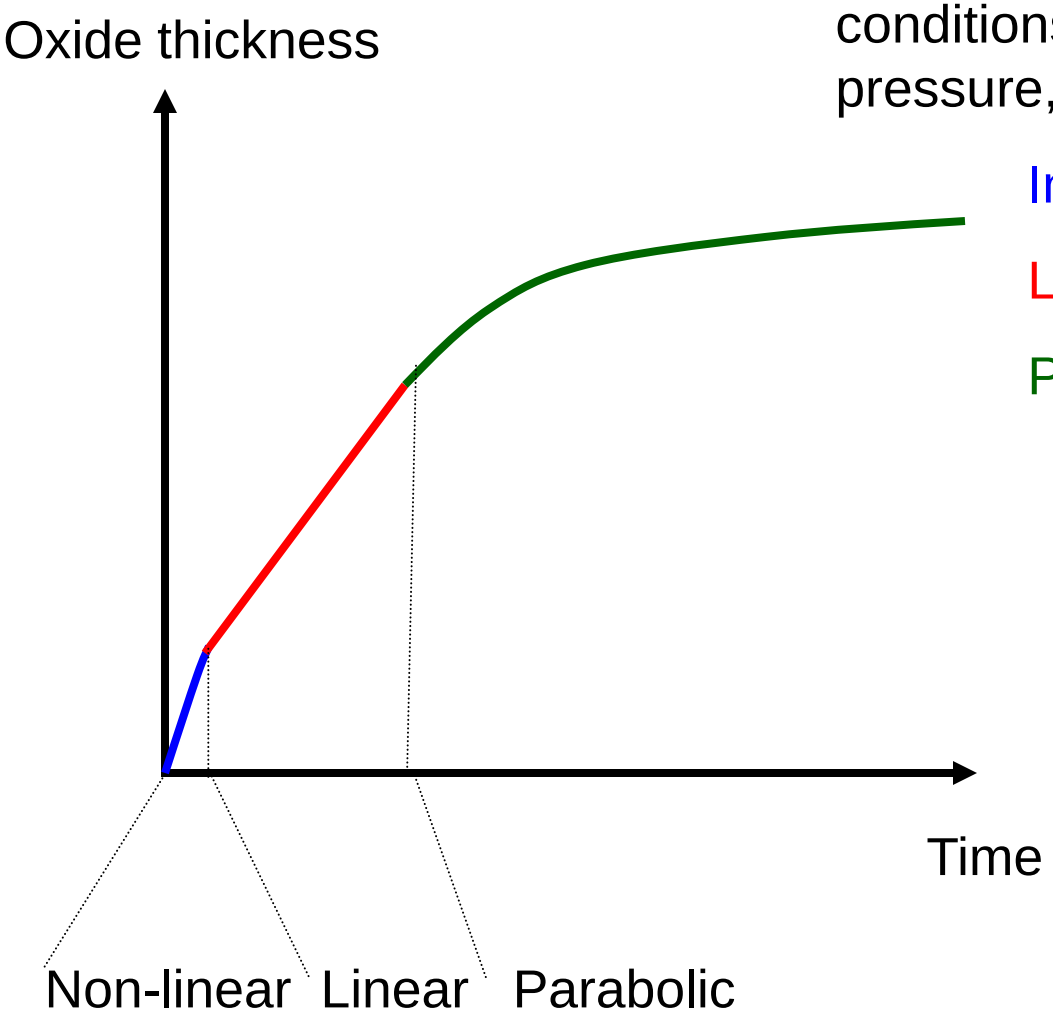
TEM of SiO_2 layer between Si substrate and polysilicon gate.



The growth of one unit thickness of oxide consumes 0.44 units of the silicon substrate.

Growth of thermal oxide

Oxide growth characteristic under fixed conditions (temperature, oxygen pressure, silicon orientation, etc).

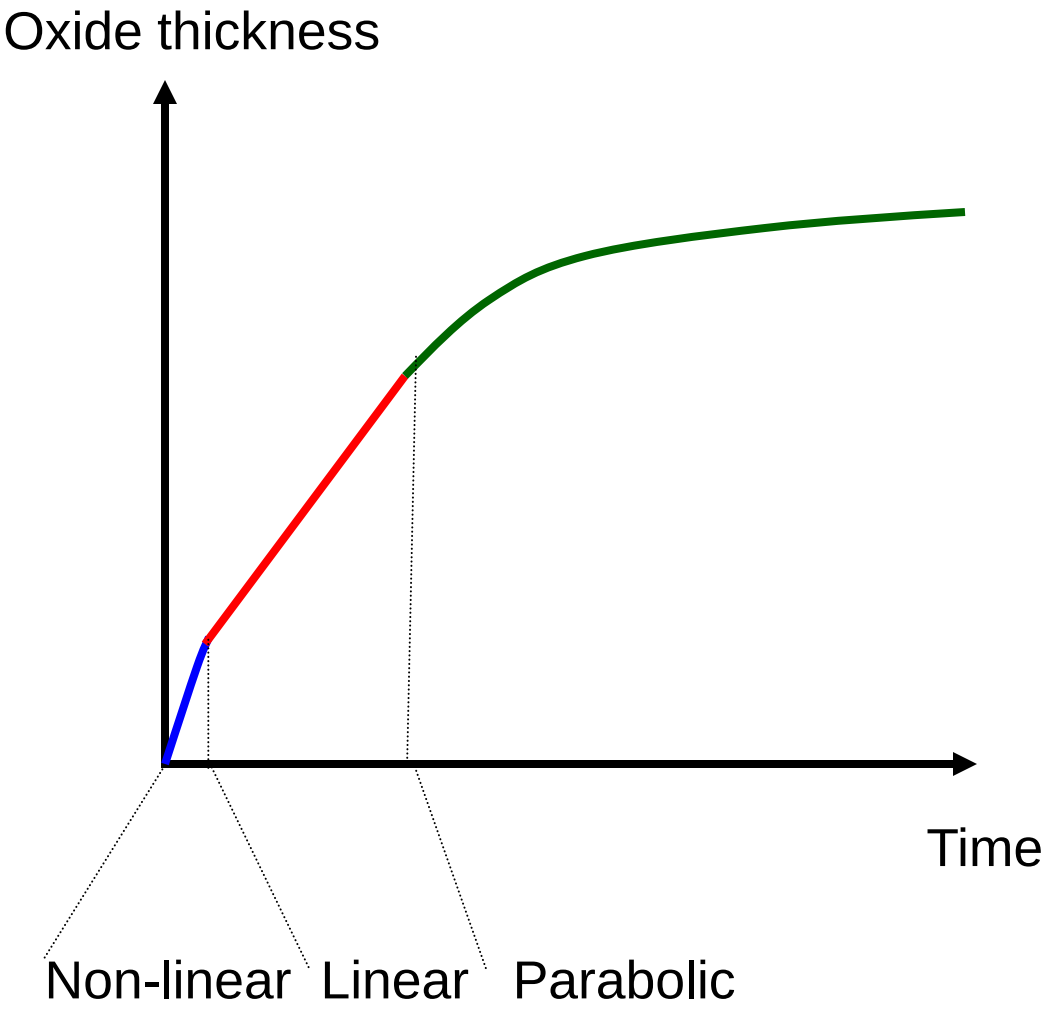


Initial non-linear section

Linear section

Parabolic section

Growth of thermal oxide

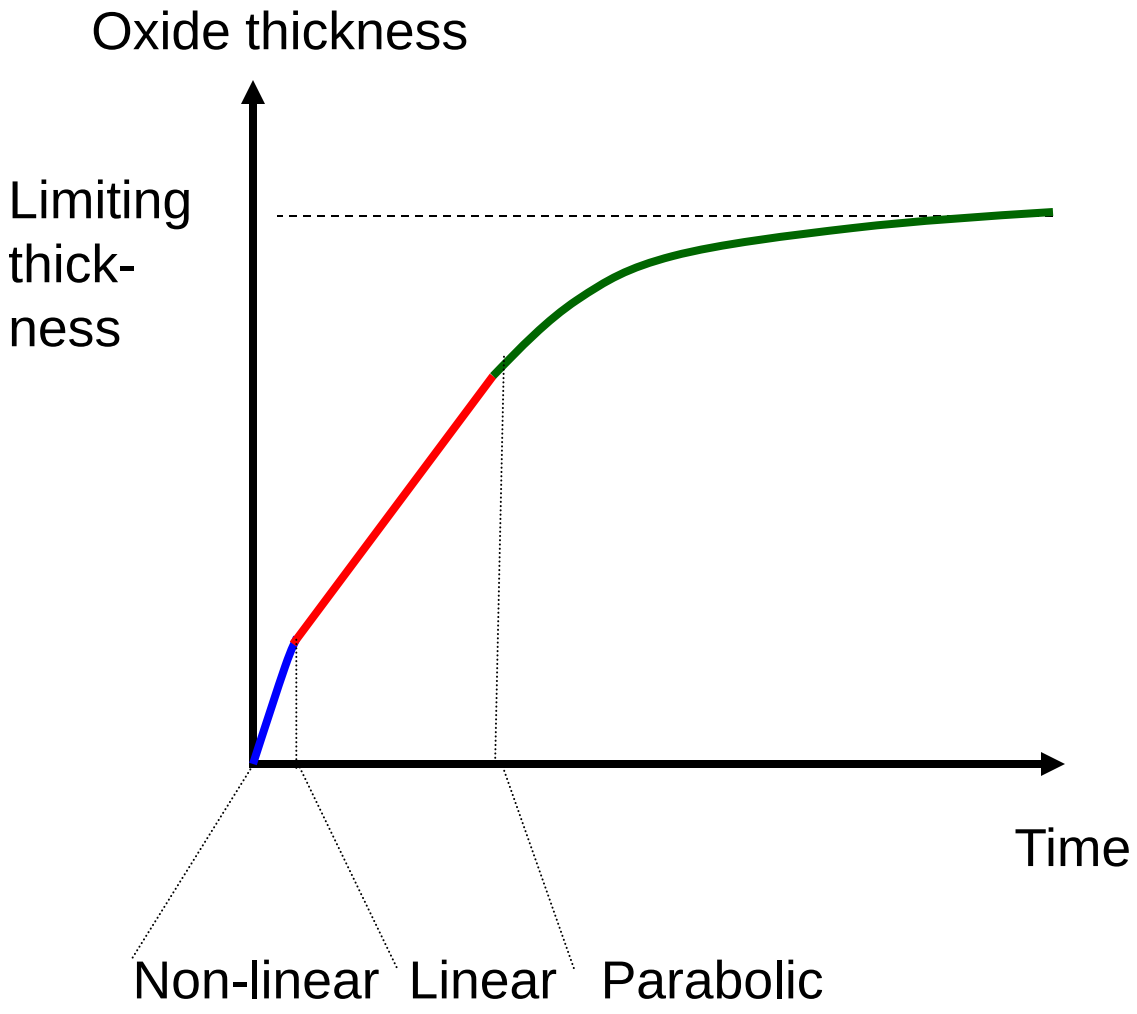


Initial part establishing equilibrium in diffusion processes.

Linear part reaction rate limited.

Parabolic part diffusion limited.

Growth of thermal oxide



Practical limiting thickness due to parabolic section.

Thickness increased by increasing temperature or using water vapour instead of oxygen.

Analytical description due to Deal and Grove.

Worked example

Silicon is thermally oxidised under conditions that yield rate coefficients of A=0.35μm and B=0.015 μm^2/hr.

If the initial oxide thickness was 0.1 μm, how much silicon will have been consumed after 3hrs of oxidation?

The oxide thickness is given by

$$t_{ox}^2 + At_{ox} = B(t + \tau) \qquad \tau = \frac{t_0^2 + At_0}{B}$$

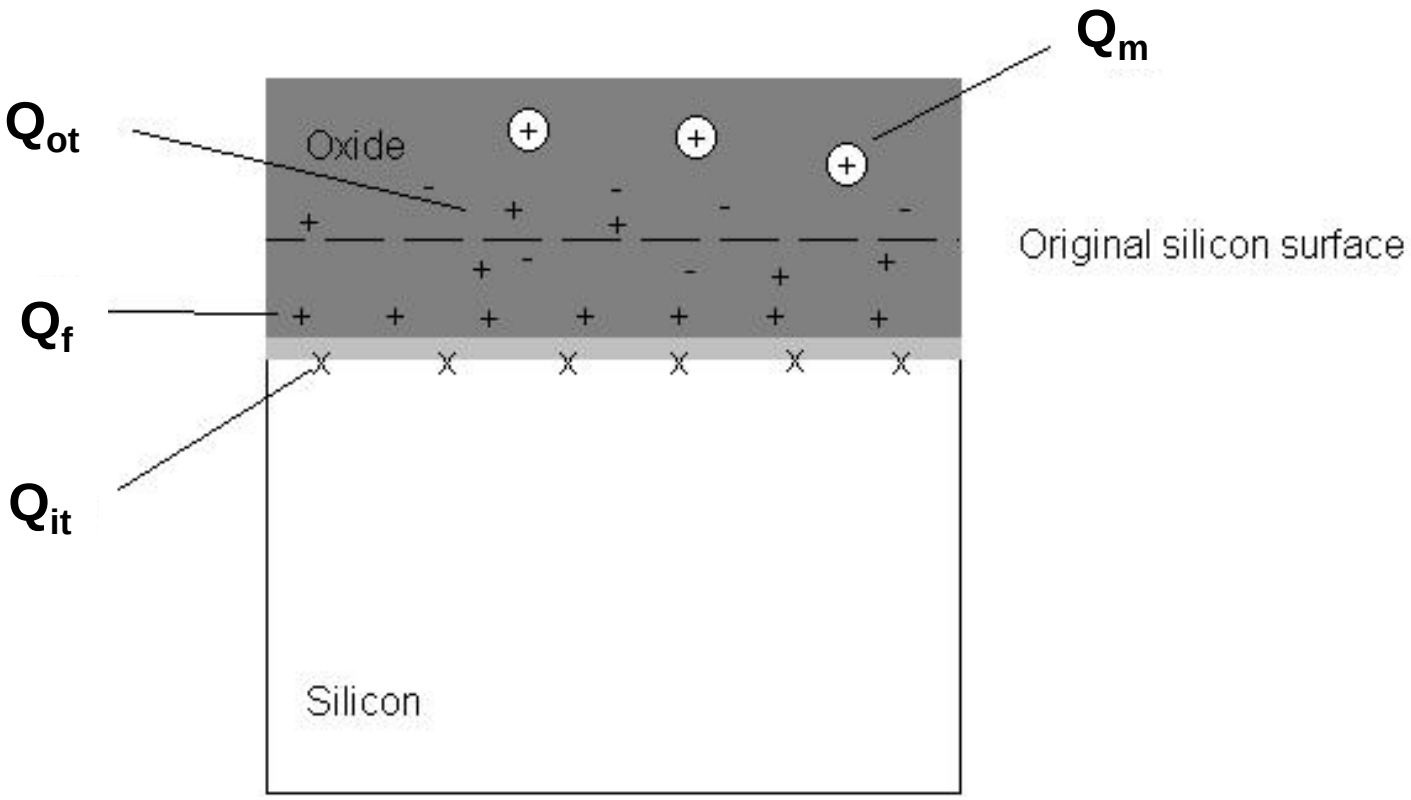
Worked example

Substituting we get for $\tau = (0.1^2 + 0.35 \times 0.1)/0.015 = 3$hrs.

So that $t_{ox}^2 + 0.35t_{ox} = 0.015$ (3+3) i.e. taking the positive root $t_{ox} = 0.17\mu$m.

The increase in the oxide thickness is 0.17-0.10 = 0.07 μm, so that the thickness of silicon consumed was 0.44 x 0.07 = 0.031μm.

Charge present in oxide layer



Q_m	mobile ionic charge.
Q_{ot}	oxide trapped charge
Q_f	fixed oxide charge
Q_{it}	interface trapped charge

Mobile ionic charge Q_m

Alkali ions are highly mobile within the oxide even at device operating temperatures.

Amount of charge depends on processing and environmental conditions.

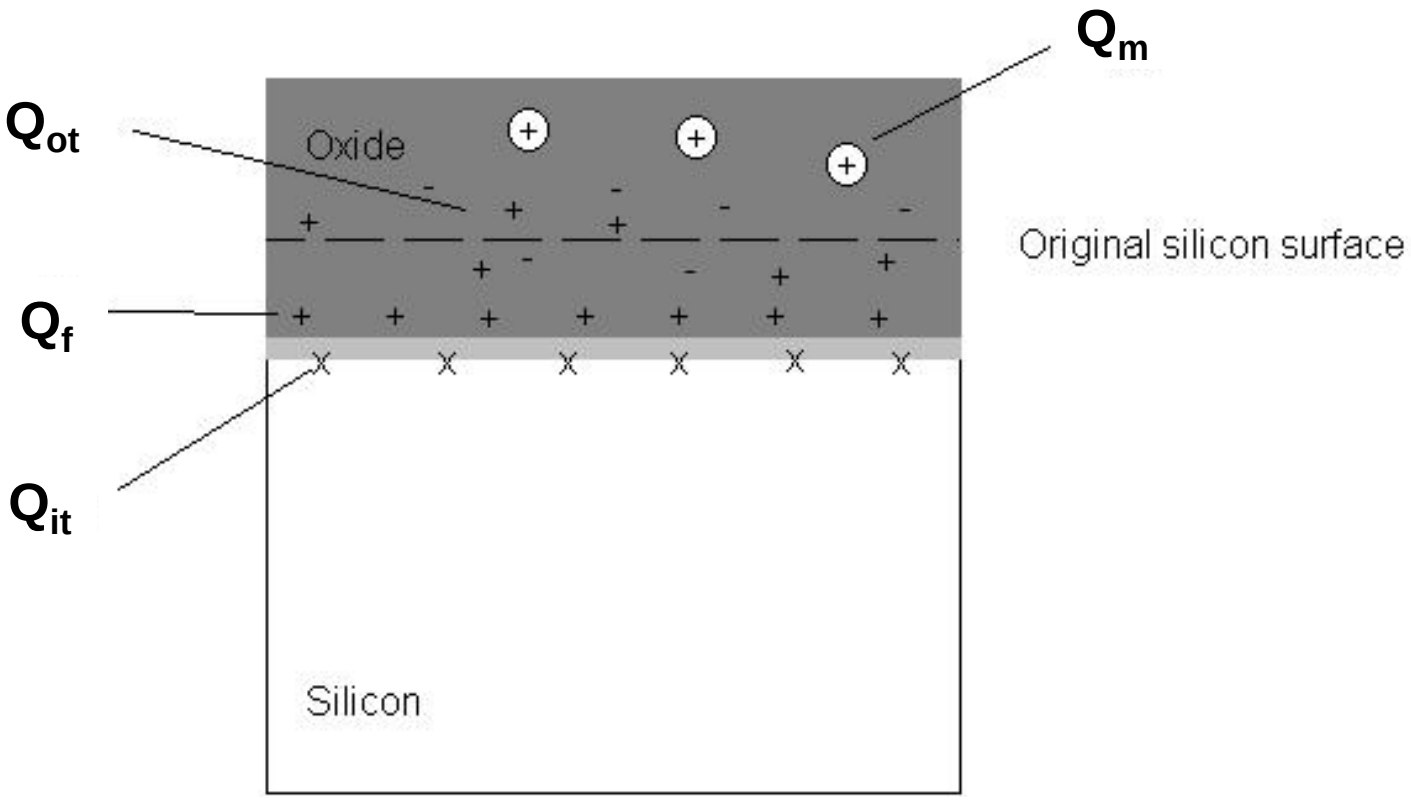
Position of the charge depends on operating history and can be changed through the application of electric fields.

Due to this variability, devices based on MOS structures could not be implemented in practice until this source of charge was controlled.

Alkali ions can come from the materials used to fabricate the structure (an early source was from the tungsten filament used to evaporate the aluminium gate metal) or from fingerprints.

Clean processing and efficient device encapsulation are used to control this problem.

Charge present in oxide layer



Q_m	mobile ionic charge
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Oxide trapped charge Q_{ot}

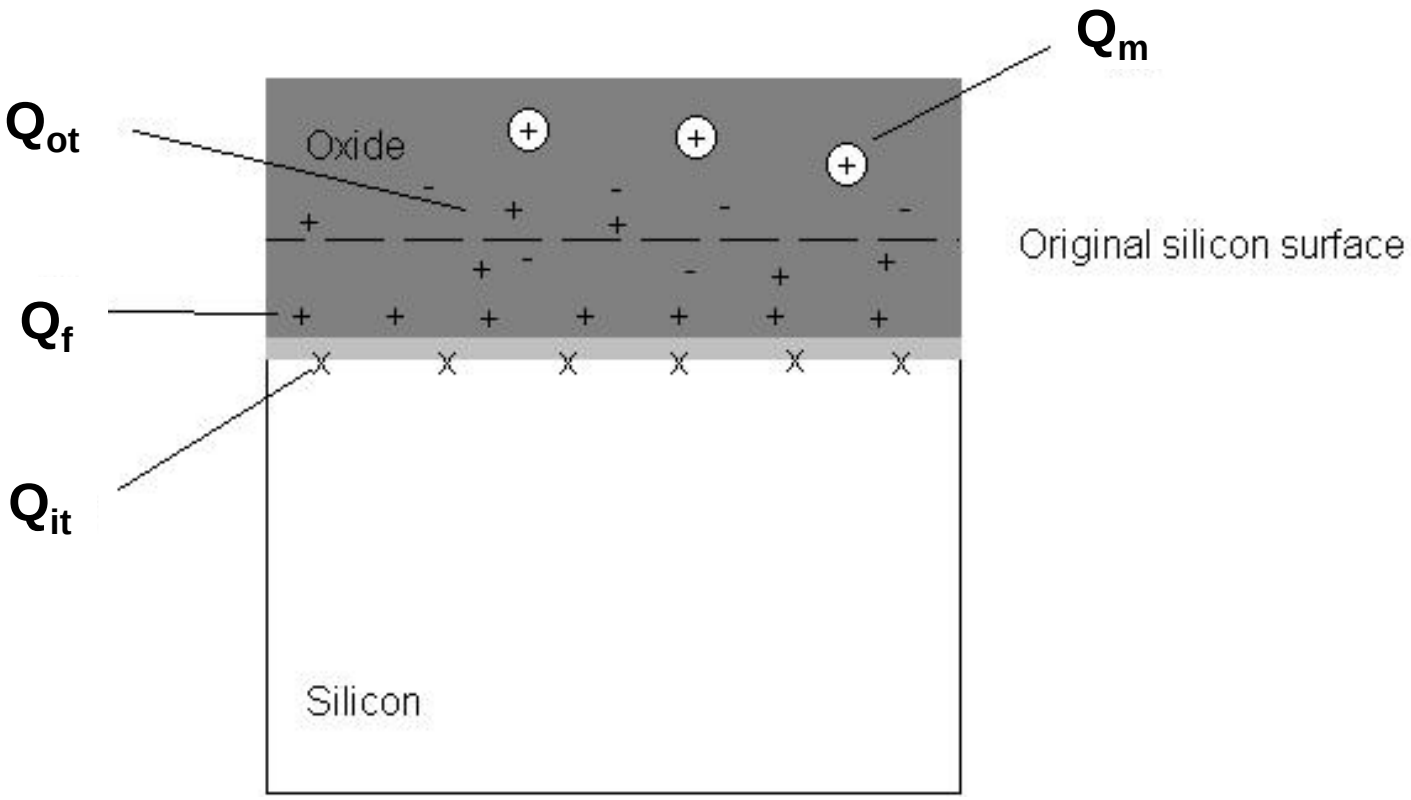
Ionising radiation can generate electron-hole pairs in the oxide layer which become trapped.

Similarly, hot carriers from the substrate can contribute to this charge.

The origin of these traps is due to processing during device fabrication, particularly ion implantation, RIE etching, electron beam evaporation, wet oxidation, lithography, etc.

Traps are characterised by their capture cross-section which decreases with increasing temperature and oxide field.

Charge present in oxide layer



Q_m	mobile ionic charge
Q_{ot}	oxide trapped charge
Q_f	fixed oxide charge
Q_{it}	interface trapped charge

Fixed oxide charge Q_f

SiO_2 found to contain unavoidable positive charge associated with the growth of the oxide.

At the interface a region (~1nm) consists of SiO_x rather than SiO_2.

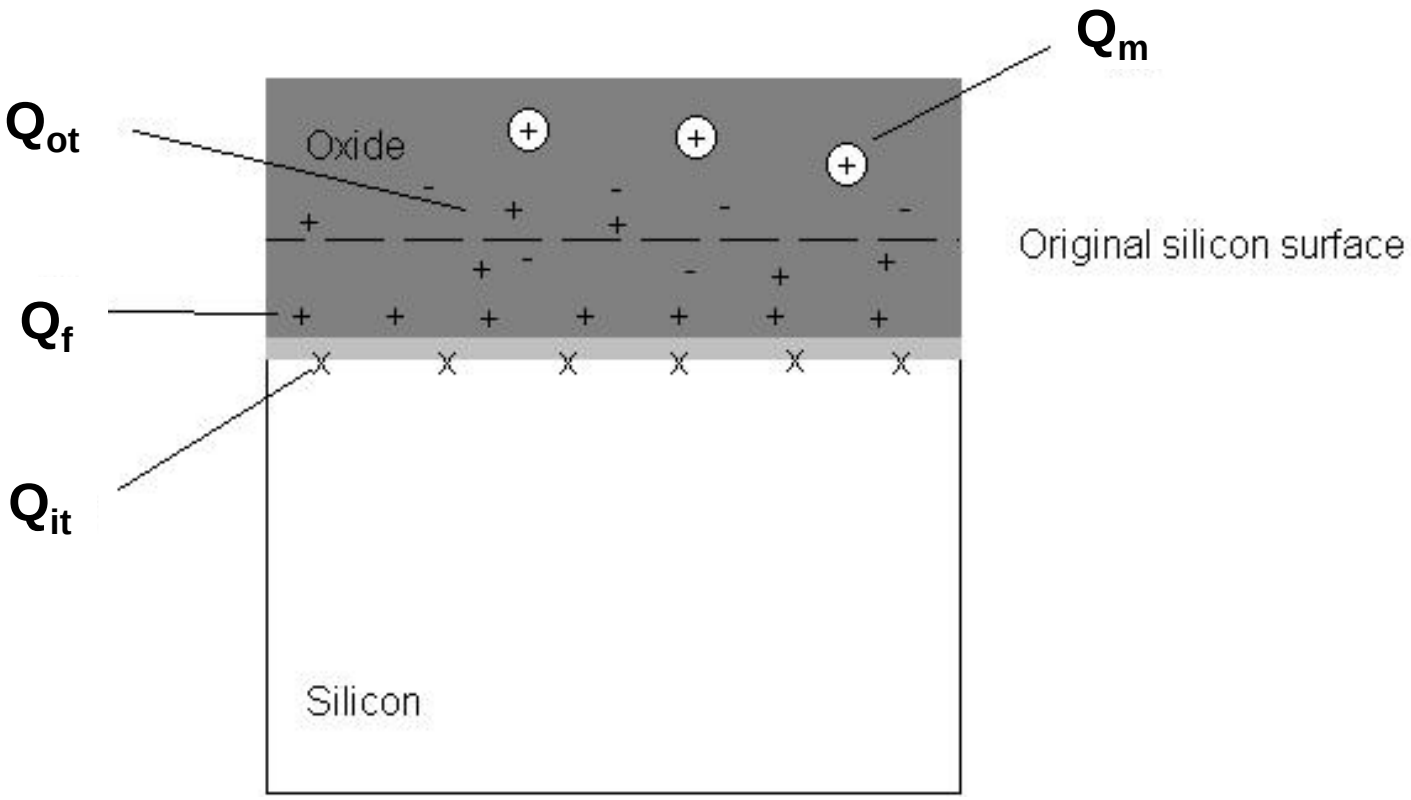
Leads to additional charge $\mathbf{Q_f}$ close to the interface; amount of charge depends on the substrate orientation and oxide growth conditions.

Fixed oxide charge density depends on substrate orientation in the following manner:

(100) < (110) < (111)

So that (100) oriented substrates are most commonly used for MOS processing.

Charge present in oxide layer



Q_m	mobile ionic charge
Q_{ot}	oxide trapped charge
Q_f	fixed oxide charge
Q_{it}	interface trapped charge

Interface trapped charge Q_{it}

Unsatisfied or dangling bonds at oxide-silicon interface, with loosely bound electrons, are the origin of surface states.

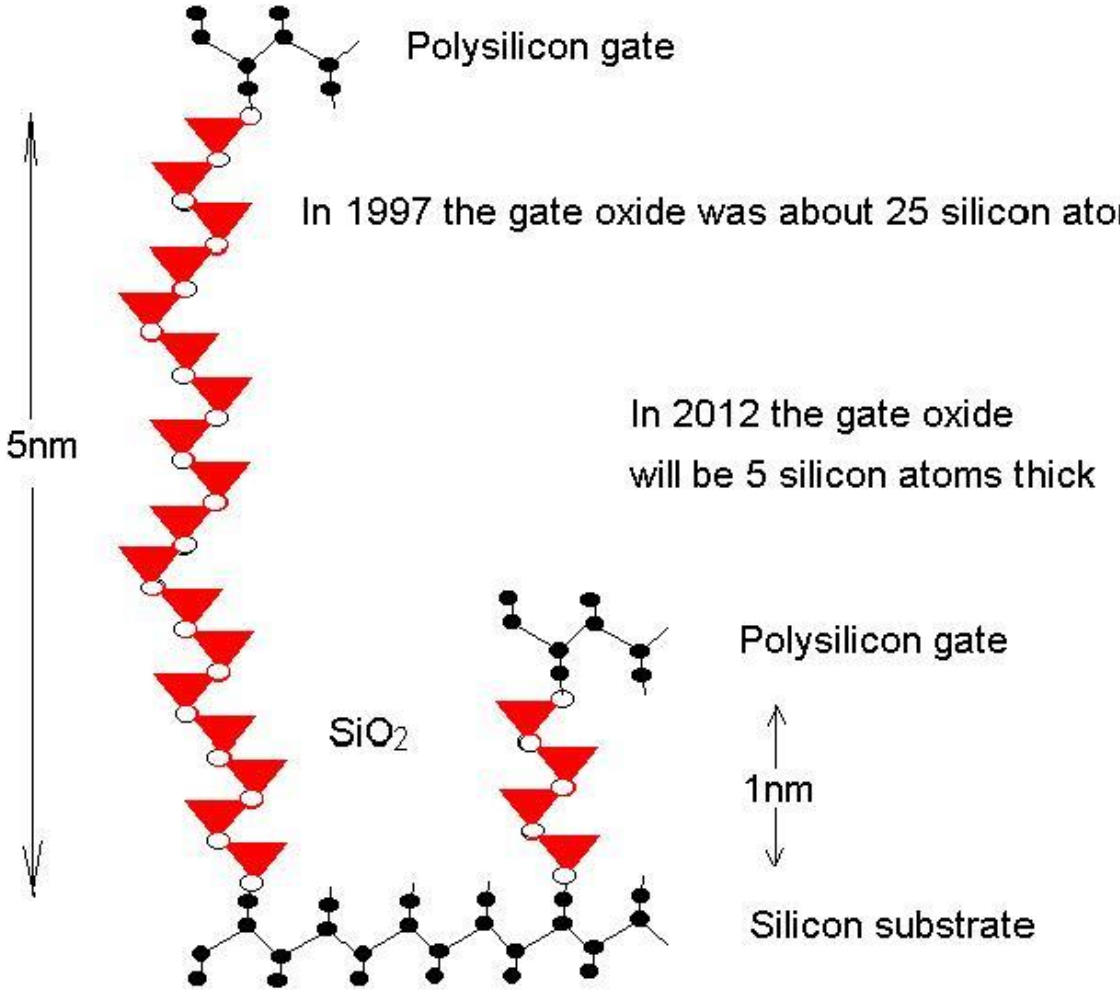
Expected to behave like donors i.e. they carry a positive charge when the electron escapes the bond.

However, simple picture modified by rearrangement so that both donor-like and acceptor-like states are realised.

If in good communication with a source (and sink) of carriers then the surface potential is modified by their presence.

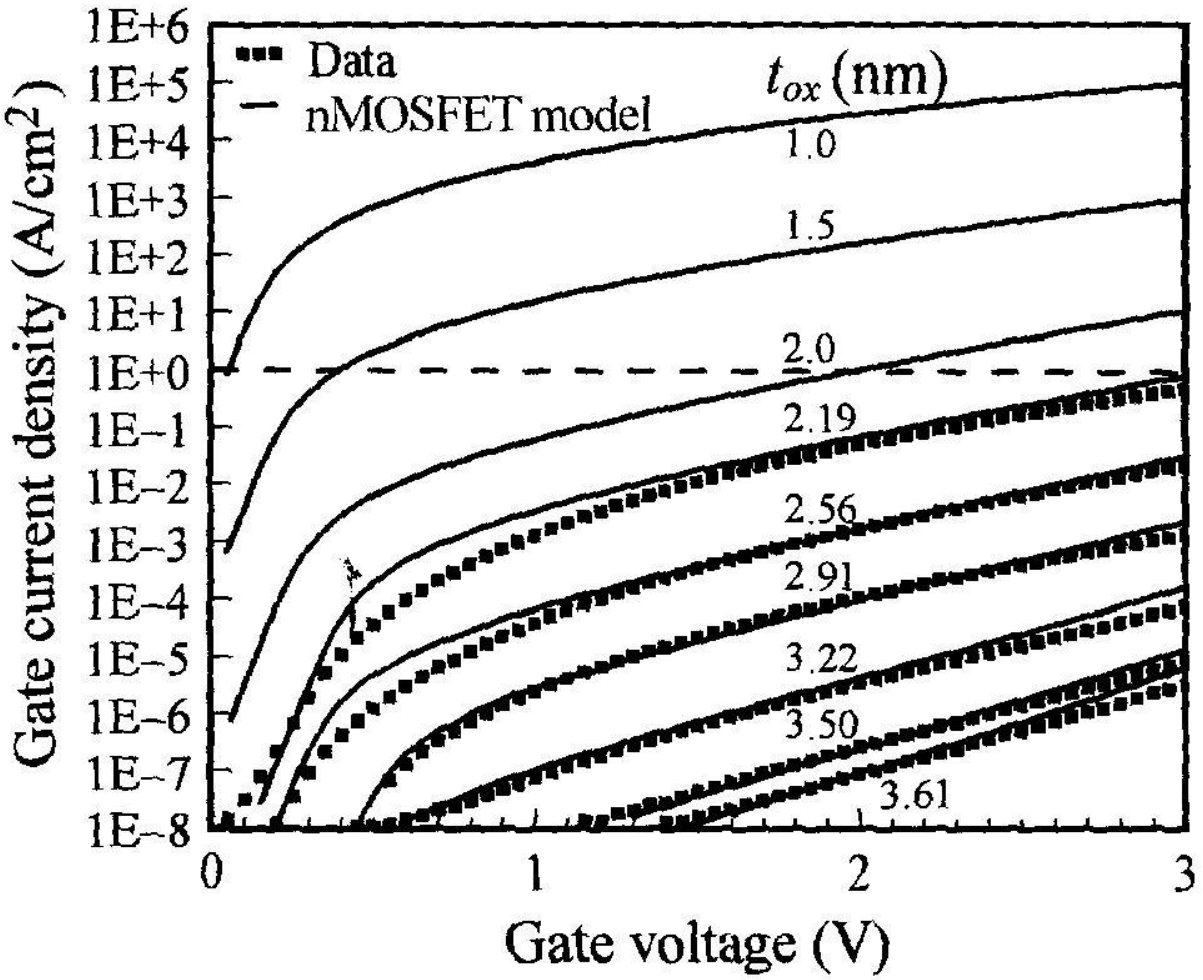
States have a range of time constants ranging from fast to slow and are associated with flicker noise.

Ultra-thin oxides



Oxide layer now getting so thin that we cannot ignore that it is made up of atoms of silicon and oxygen.

Gate oxide leakage

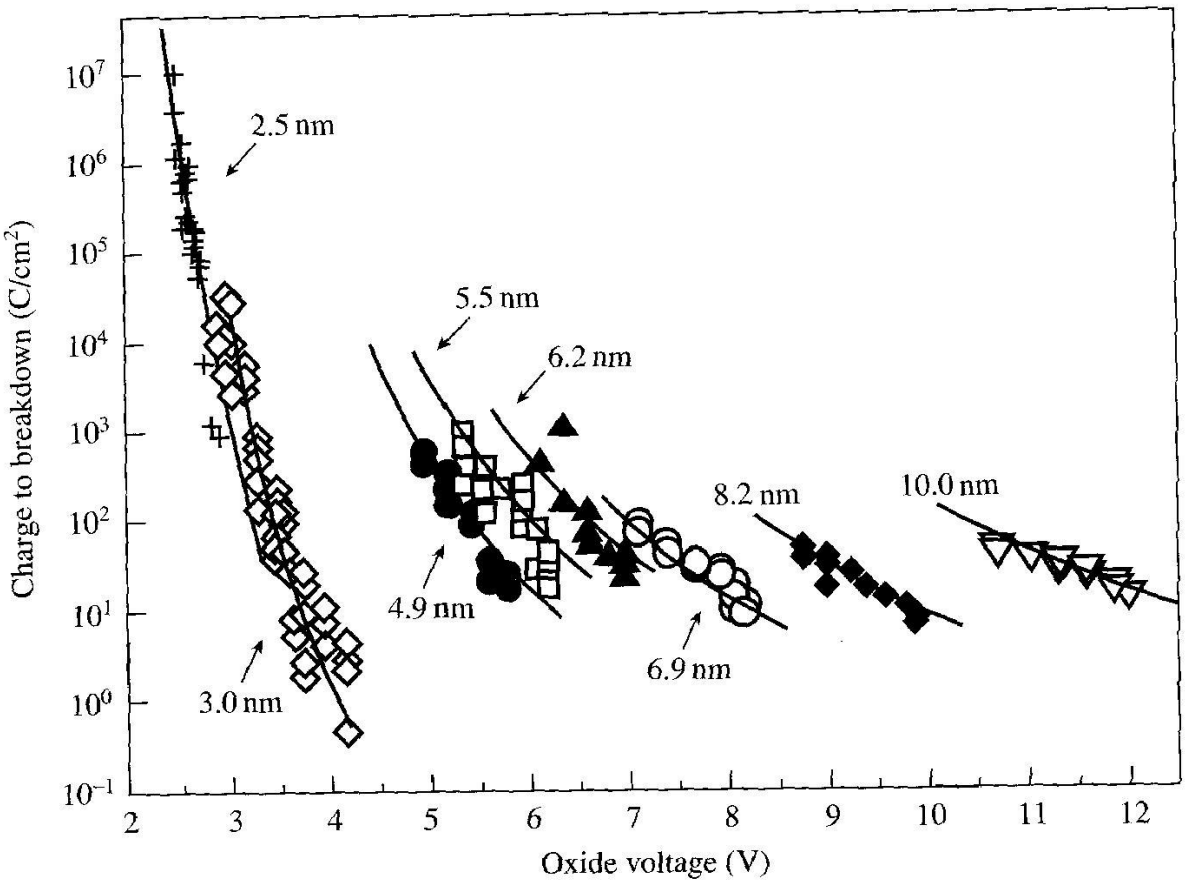


When a barrier thickness approaches a few nm s tunnelling becomes very likely.

Such very thin oxide layers are very leaky!

When this current density reaches about 1 A cm^{-2} the device will no longer work.

Charge to breakdown



Thinner oxides are also more prone to failure.

Gate oxides are used with electric fields very close to the breakdown limit.

Equivalent oxide thickness

The phrase equivalent oxide thickness, t_{eq}, refers to the thickness of any dielectric scaled by the ratio of its dielectric constant to that of silicon dioxide (where $\varepsilon_{SiO2} = 3.9$) such that

$$t_{eq} = \frac{3.9}{\varepsilon_{dielectric}} t_{SiO_2}$$

The concept of an equivalent oxide thickness will be used later on when non-ideal effects modify the behaviour of a dielectric film.

Roadmap for equivalent dielectric thickness

Production year	Minimum feature size (μm)	Equivalent oxide thickness (nm)
1997	0.25	4-5
1999	0.18	3-4
2001	0.15	2-3
2003	0.13	2-3
2006	0.10	1.5-2
2009	0.07	<1.5
2012	0.05	<1.0

Source IBM